

# CB-1 SWG LOGIC SCHEMATICS

001.TITLE PAGE  
 002.EC HISTORY  
 003.CPU(1/16) : DDI/EDP  
 004.CPU(2/16) : MISC/JTAG  
 005.CPU(3/16) : DDR3L CHANNEL-A  
 006.CPU(4/16) : DDR3L CHANNEL-B  
 007.CPU(5/16) : RTC/HDA/SATA/JTAG  
 008.CPU(6/16) : CLOCK SIGNALS  
 009.CPU(7/16) : LPC/SPI/SMBUS/C-LINK  
 010.CPU(8/16) : SYSTEM PM  
 011.CPU(9/16) : LCD/PCI/DDI CONTROL  
 012.CPU(10/16) : GPIO/CPU/MISC/LPIO  
 013.CPU(11/16) : PCIE/USB  
 014.CPU(12/16) : POWER  
 015.CPU(13/16) : POWER  
 016.CPU(14/16) : GND  
 017.CPU(15/16) : NCTF  
 018.CPU(16/16) : CFG/RESERVED  
 019.DDI-VGA CONVERTER  
 020.BLANK  
 021.XDP CONNECTOR  
 022.RTC BATTERY  
 023.SPI FLASH  
 024.DDR3L BASE MEMORY CH-A (1/2)  
 025.DDR3L BASE MEMORY CH-A (2/2)  
 026.DDR3L SO DIMM CHANNEL-B  
 027.DDR3L DECOUPLING  
 028.N14M-GE(1/6) : PEG I/F  
 029.N14M-GE(2/6) : DIGITAL OUT I/F  
 030.N14M-GE(3/6) : VRAM I/F  
 031.N14M-GE(4/6) : GPIO  
 032.N14M-GE(5/6) : POWER  
 033.N14M-GE(6/6) : GND  
 034.VRAM CHANNEL-A  
 035.BLANK

36.MEMORY TERMINATION  
 37.BLANK  
 38.LCD CONNECTOR  
 39.BLANK  
 40.EXT CRT INTERFACE  
 41.DISPLAY PORT CONNECTOR  
 42.BLANK  
 43.SATA HDD CONN  
 44.BLANK  
 45.USB POWER/CONN  
 46.GBE CLARKVILLE  
 47.BLANK  
 48.GBE MAGNETICS  
 49.RJ45 CONNECTOR  
 50.PCIE MINI CARD SLOT  
 51.MEDIA CARD CONTROLLER  
 52.MEDIA CARD INTERFACE  
 53.SMART CARD I/F  
 54.AUDIO ALC3232-GR  
 55.AUDIO CONNECTOR  
 56.AUDIO JACK SENSE  
 57.AUDIO EXT MIC I/F  
 58.AUDIO SPEAKER  
 59.AUDIO BEEP  
 60.BLANK  
 61.MEC1619(1/3)  
 62.MEC1619(2/3)  
 63.MEC1619(3/3)  
 64.KEYBOARD CONNECTOR  
 65.TOUCH PAD CONNECTOR  
 66.BLANK  
 67.FAN CONNECTOR  
 68.G-SENSOR  
 69.TPM  
 70.EEPROM/SMBUS SW

ST-1  
 VER0.1  
 June/19/2012


71.THINK ENGINE(1/2)  
 72.THINK ENGINE(2/2)  
 73.DC-IN  
 74.BATTERY INPUT  
 75.BATTERY CHARGER(BQ24760)  
 76.CHARGER SELECTOR  
 77.BATTERY MONITOR  
 78.DC/DC VCC5M/VCC3M (TPS51220A)  
 79.DC/DC VCCCPUCORE(VT1320M)  
 80.DC/DC VCCCPUCORE(VT1334S)  
 81.BLANK  
 82.VCCCPUCORE DECOUPLING  
 83.DC/DC VCCGFXCORE\_D (TPS51728)  
 84.BLANK  
 85.DC/DC VCC1R05AMT(VT356)  
 86.DC/DC VCC1R35A(VT357)  
 87.DC/DC VCC0R675B(TPS51200)  
 88.DC/DC VCC1R5VIDEO(VT356)  
 89.DC/DC VCC1R05VIDEO\_PLL(BD3551HFN)  
 90.DC/DC VCC1R8B(BD9139)  
 91.BLANK  
 92.DC/DC VCC1R5B(BD3551HFN)  
 93.LOAD SW PCH SUS  
 94.LOAD SW LAN  
 95.LOAD SW VIDEO  
 96.LOAD SW B  
 97.BLANK  
 98.LOAD SW WWAN & WLAN  
 99.PTH FOR SCREW HOLES  
 100.3rd USB

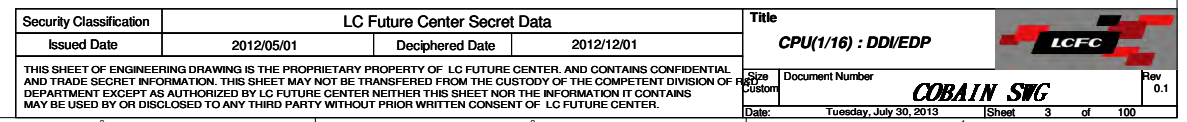
## EC Modify History

Date	EC version	File name
2013/05/06	CB_1_SWG_SIT_EC001-005	JV_CB-1_SWG_SIT_SCH_EC001-005_050601.pdf
2013/05/07	JVCB-1_SWG_SIT-SWG_ECR001-002	JV_CB-1_SWG_SIT_SCH_EC001-005_050701.pdf
2013/05/09	JVCB-1_SWG_SIT-SWG_ECR003	JV_CB-1_SWG_SIT_SCH_EC001-005_050901.pdf
2013/05/10	JVCB-1_SWG_SIT-SWG_ECR004	JV_CB-1_SWG_SIT_SCH_EC001-005_051001.pdf
2013/05/14	JVCB-1_SWG_SIT-SWG_ECR005	JV_CB-1_SWG_SIT_SCH_EC001-005_051401.pdf
2013/05/14	JVCB-1_SWG_SIT-SWG_EC006	JV_CB-1_SWG_SIT_SCH_EC001-006_051402.pdf
2013/07/03	JV_CB-1_SWG_SVT_SCH_EC001-004	JV_CB-1_SWG_SVT_SCH_EC001-004_070301.pdf

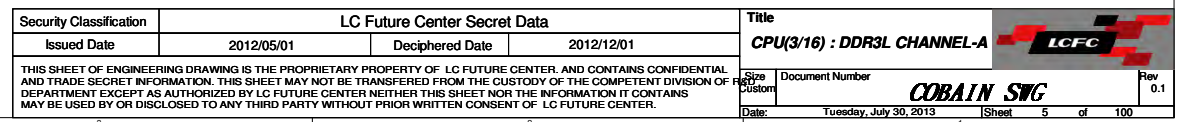
2012/10/02	CB_1_SWG_SDV_EC001-009	JV_CB-1_SWG_SDV1_SCH_EC001-008_121001A.pdf
2012/10/05	CB_1_SWG_SDV_EC010	JV_CB-1_SWG_SDV1_SCH_EC001-009_121004A.pdf
2012/10/09	CB_1_SWG_SDV_EC011	JV_CB-1_SWG_SDV1_SCH_EC009-010_100801.pdf
2012/10/12	CB_1_SWG_SDV_EC012	JV_CB-1_SWG_SDV1_SCH_EC010-011_101101.pdf
2012/10/13	CB_1_SWG_SDV_EC013	JV_CB-1_SWG_SDV1_SCH_EC011-012_101201.pdf
2012/10/16	CB_1_SWG_SDV_EC014	JV_CB-1_SWG_SDV1_SCH_EC013_101501.pdf
2012/10/17	CB_1_SWG_SDV_EC015	JV_CB-1_SWG_SDV1_SCH_EC014_101601.pdf
2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
2012/10/19	CB_1_SWG_SDV_EC017	JV_CB-1_SWG_SDV1_SCH_EC016_101801.pdf
2012/10/20	CB_1_SWG_SDV_EC018	JV_CB-1_SWG_SDV1_SCH_EC017_101901.pdf
2012/10/25	CB_1_SWG_SDV_EC018-022	JV_CB-1_SWG_SDV1_SCH_EC018-021_102401.pdf
2012/10/31	CB_1_SWG_SDV_EC023	JV_CB-1_SWG_SDV1_SCH_EC022_103001.pdf
2012/10/32	CB_1_SWG_SDV_EC023-025	JV_CB-1_SWG_SDV1_SCH_EC023-024_103101.pdf
2012/11/15	CB_1_SWG_SDV_EC025-033	JV_CB-1_SWG_SDV1_SCH_EC025-032_111401.pdf
2012/11/23	CB_1_SWG_SDV_EC033-036	JV_CB-1_SWG_SDV1_SCH_EC025-035_112201.pdf
2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	JV_CB-1_SWG_SDV_SCH_EC037-038_120401.pdf

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				Date	Tuesday, July 30, 2013

  
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Rev 0.1









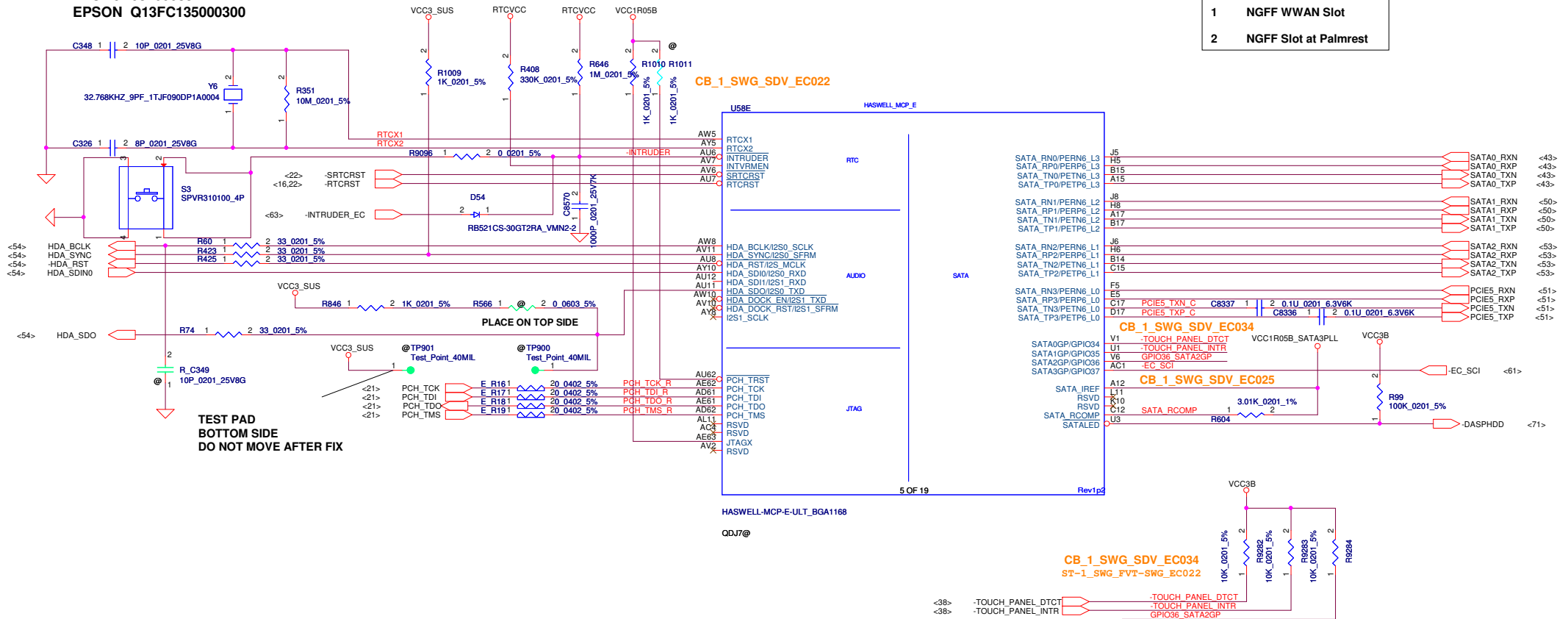


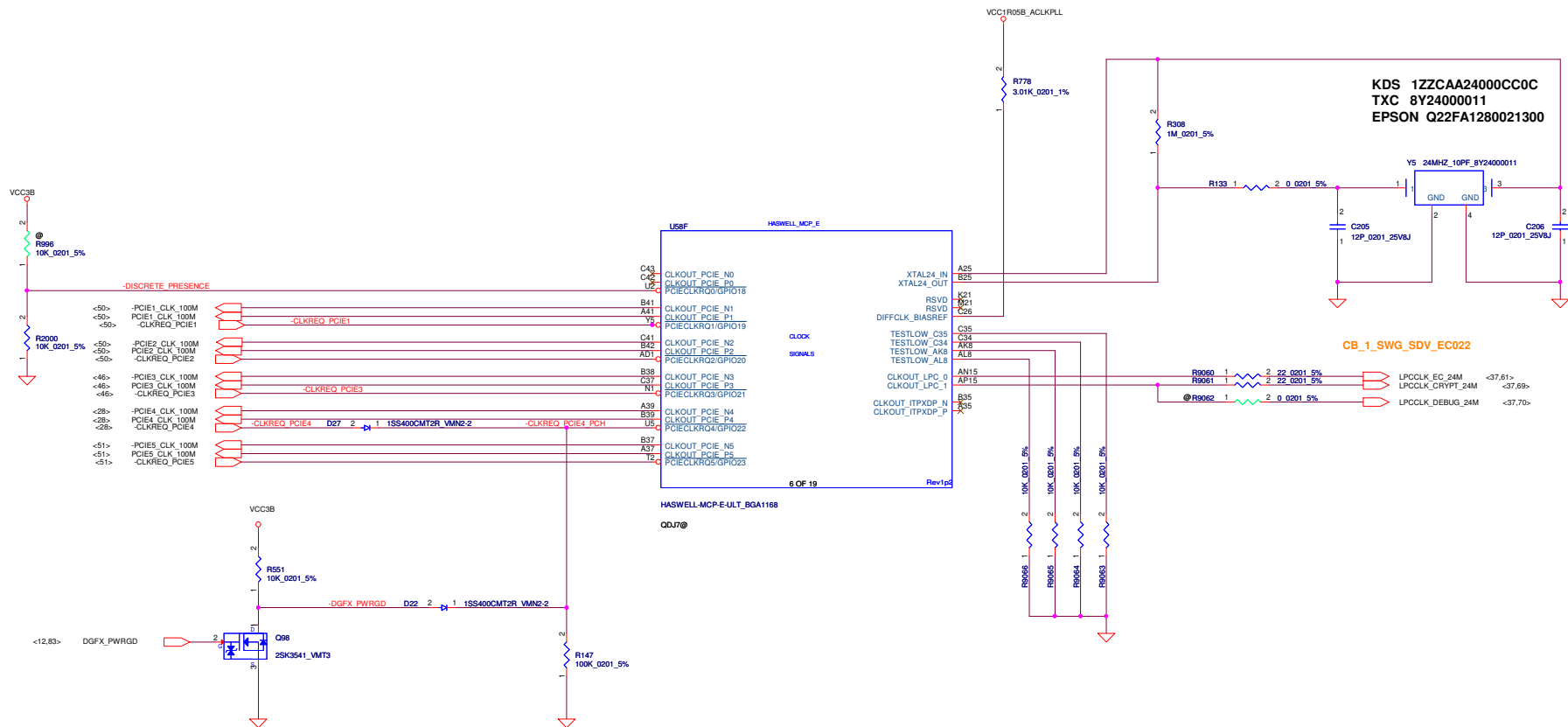
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TXC 9H03200033  
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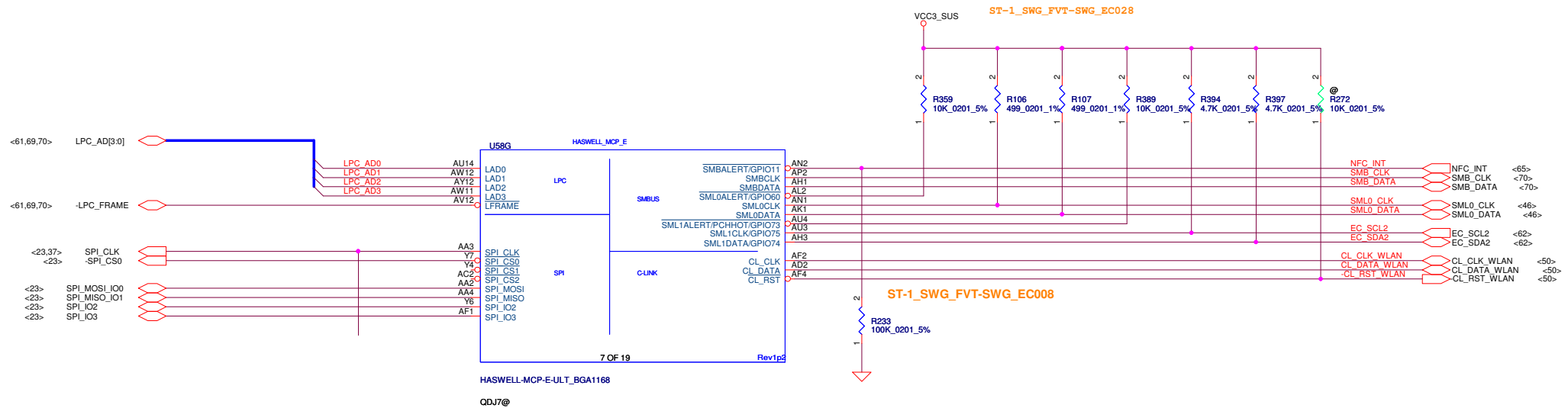
SATA Port Assignment	
0	HDD Connector
1	NGFF WWAN Slot
2	NGFF Slot at Palmrest



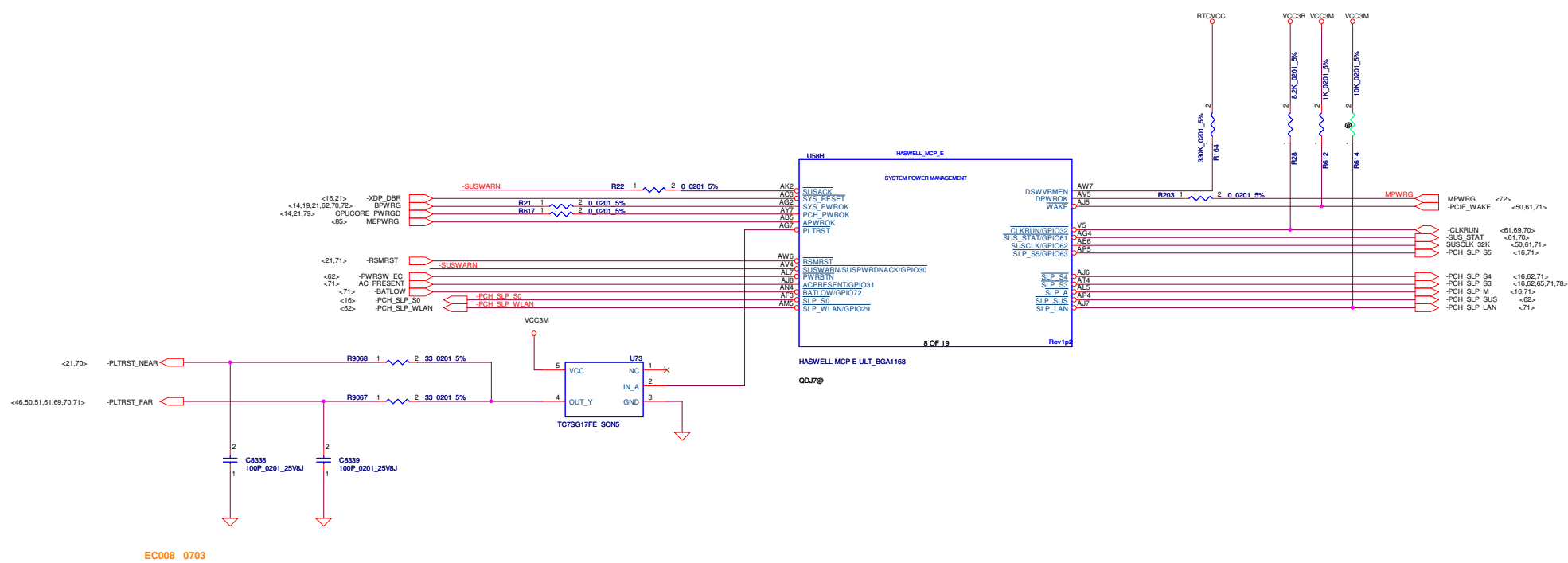


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Issued Date		Deciphered Date		CPU(6/16) : CLOCK SIGNALS						
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EC008 0703

# TABLE

CFG2 : PEG Static Lane Reversal

1 : Normal Operation  
0 : Lane Reversal

CFG4 : Display Port Presence

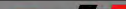
1 : Disabled  
0 : Enabled

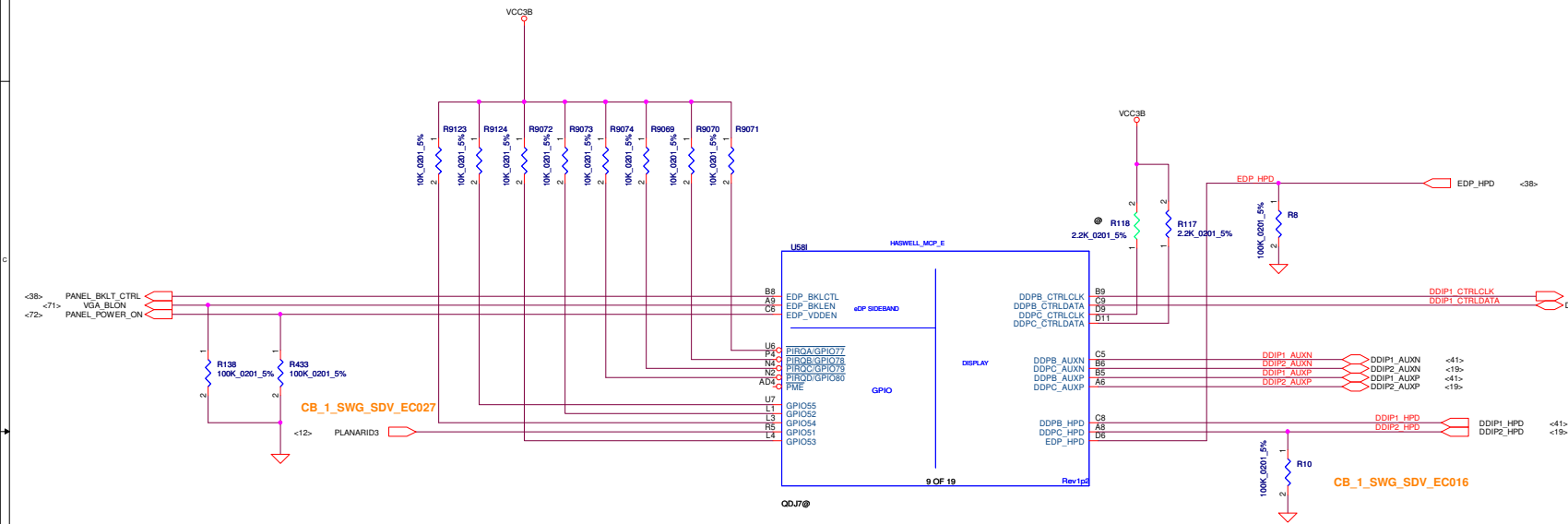
CFG[6:5] : PEG Bifurcation


11 : Func 1 Disabled, Func 2 Disabled (x16,---,---)  
10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---)  
01 : Func 1 Disabled, Func 2 Enabled  
00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

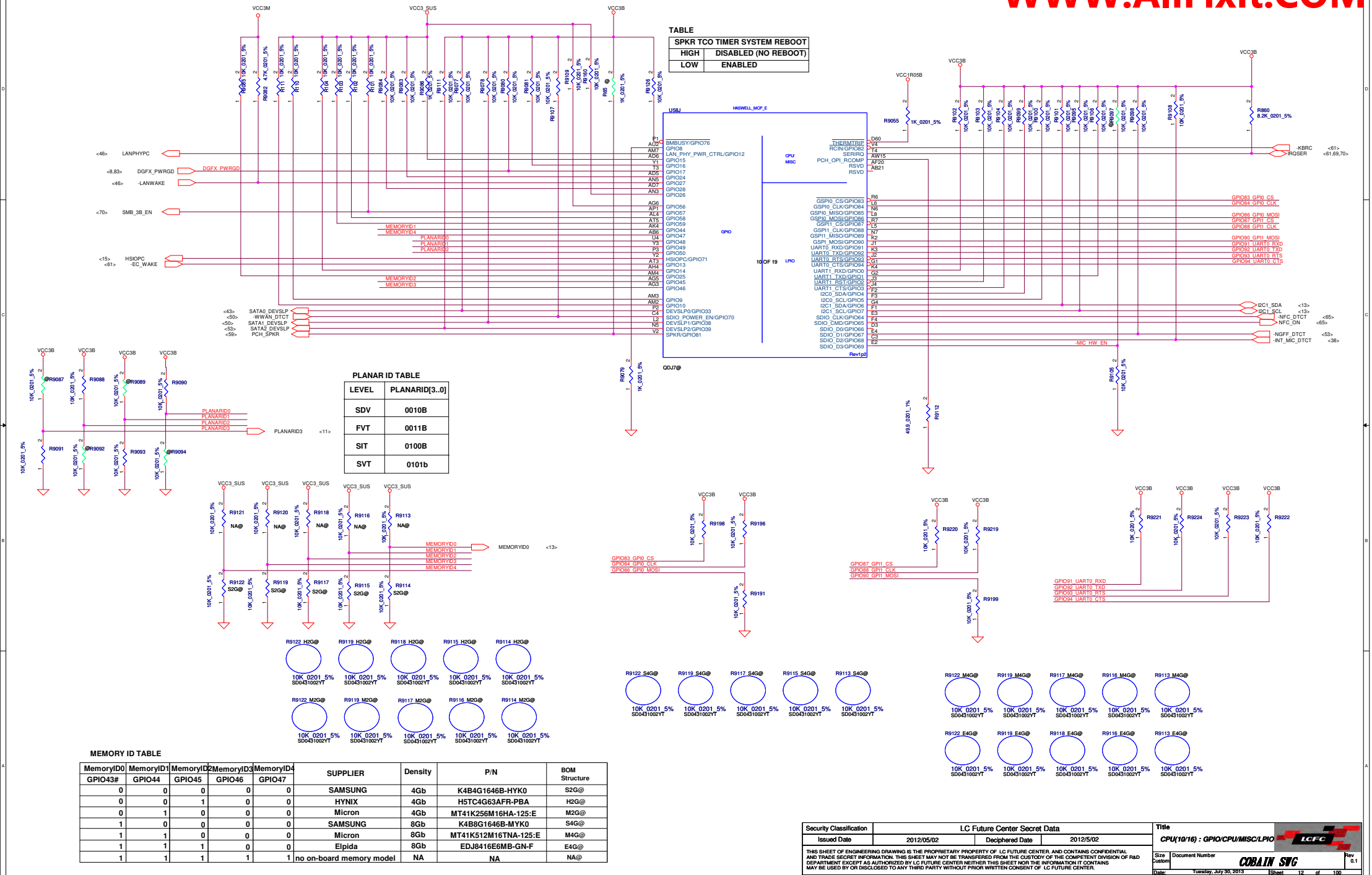
CFG7 : PEG Defer Training

1 : PEG Train Immediately Following XXRESETB Deassertion  
0 : PEG Wait for BIOS for Training

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Duration		Sheet 16		of 100		



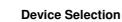
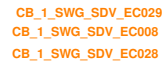
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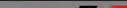


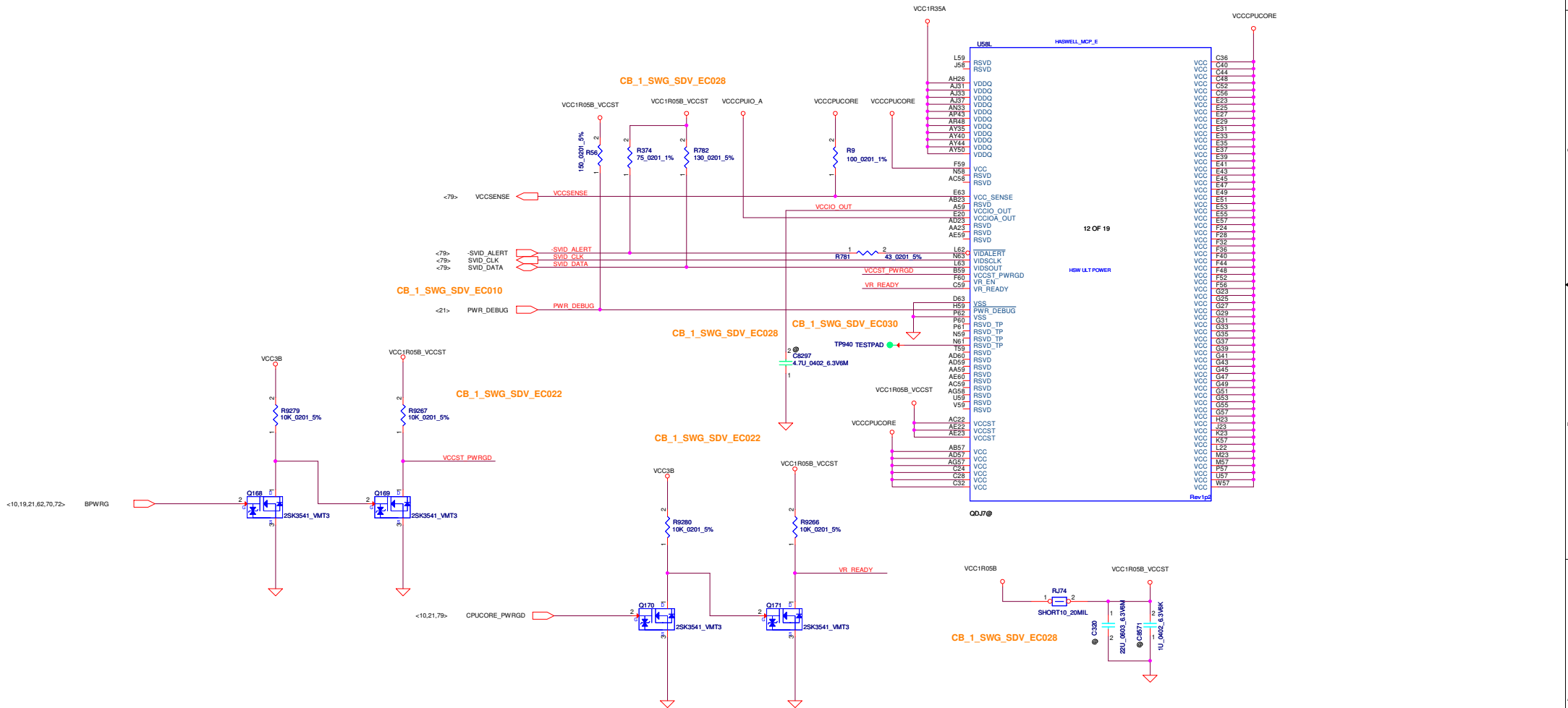
### Update PCIe Port Assignment.

CB\_1\_SWG\_SDV\_EC009

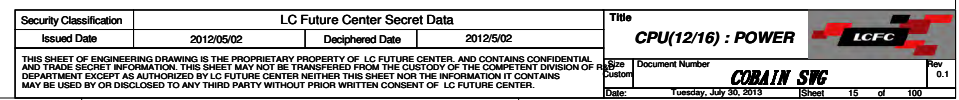
USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	USB3.0 System Port (3rd USB)



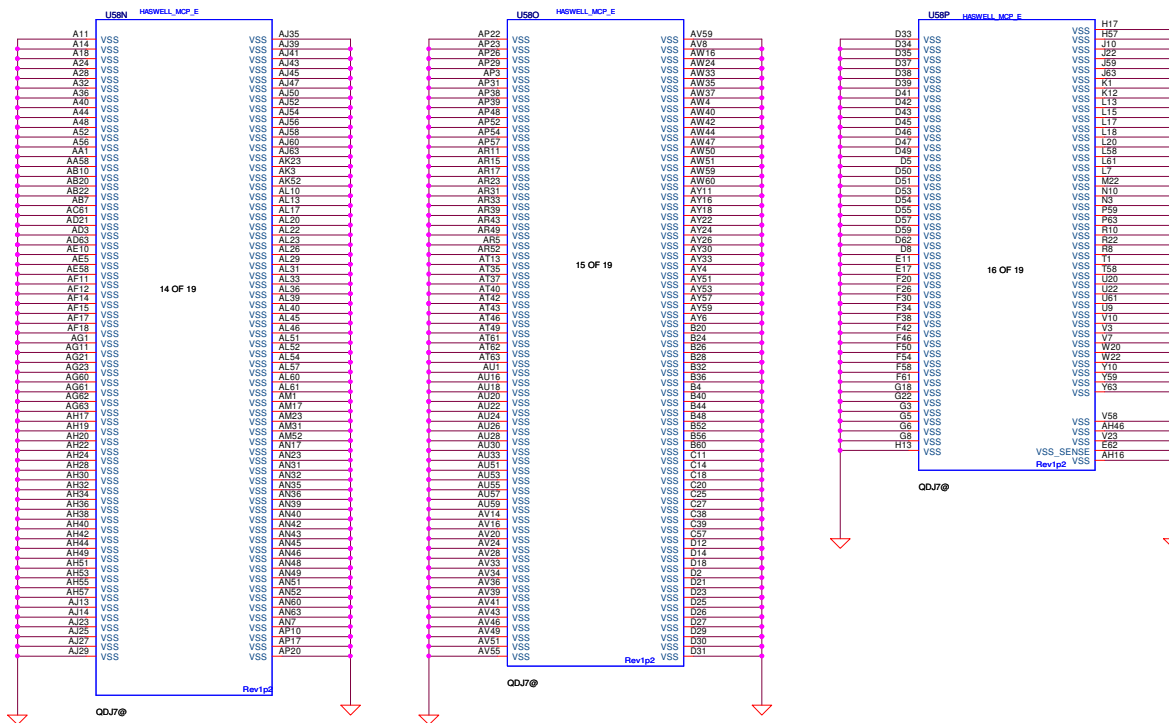
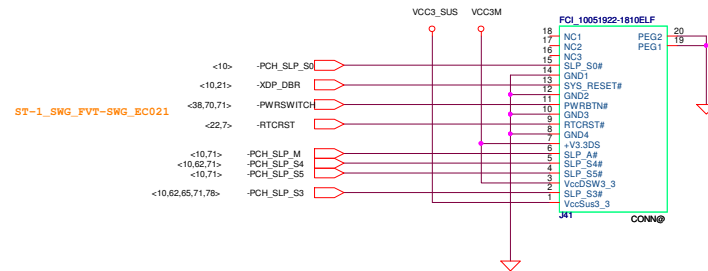
- |   |                              |                 |           |                                |                       |       |     |   |
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| Security Classification   | LC Future Center Secret Data |                 |           | Title                          | CPU(11/16) : PCIE/USB |       |     |  |
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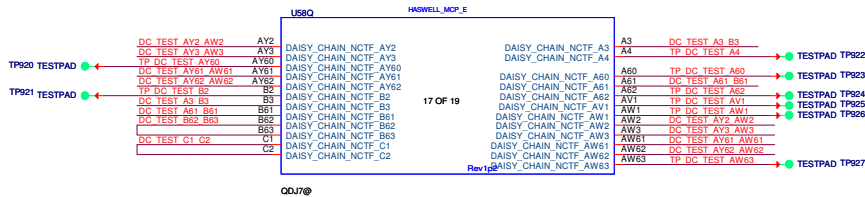
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Date		Tuesday, July 30, 2013		Sheet 14 of 100	



# APS/PETS Interface



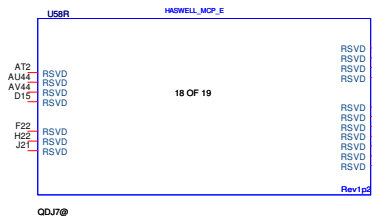
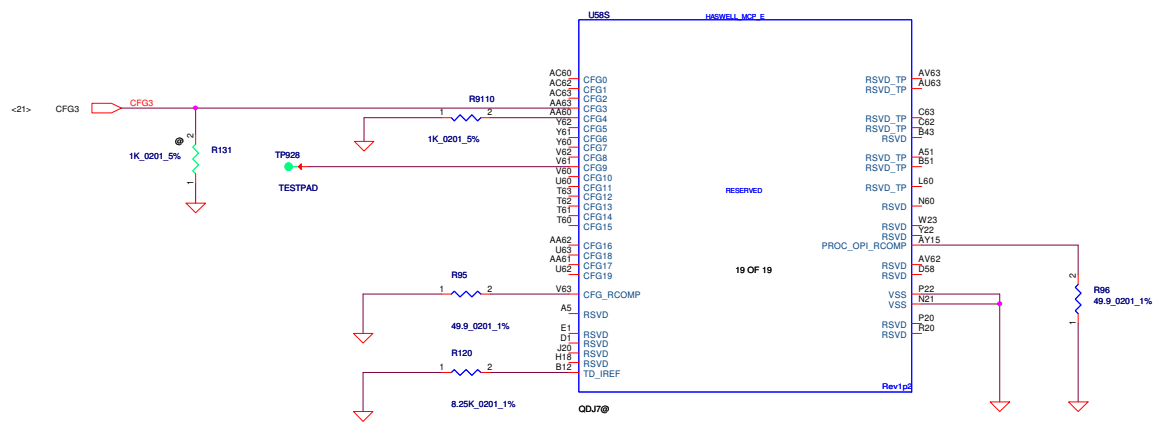


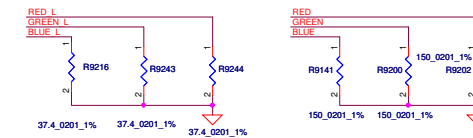



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				Sheet	17 of 100

Table


CFG4: Display Port Presence
1: Disabled
0: Enabled





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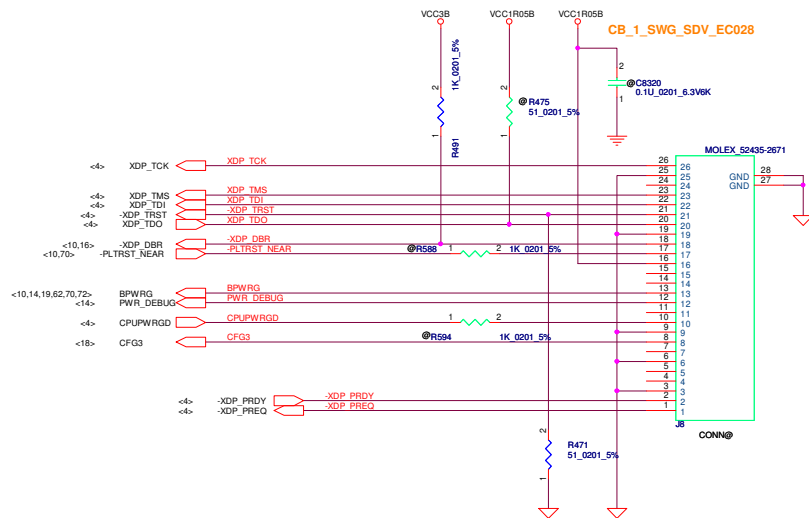


TABLE NOTE: J8 "ASM" FOR PDV/SDV ONLY.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R475	ASM	NO ASM
TRST#	R471	ASM	ASM
DBRST#	R491	ASM	ASM
RESET#	R588	ASM	NO ASM
PWRGD	R594	ASM	NO ASM
	J8	ASM	NO ASM

↑  
LOGIC

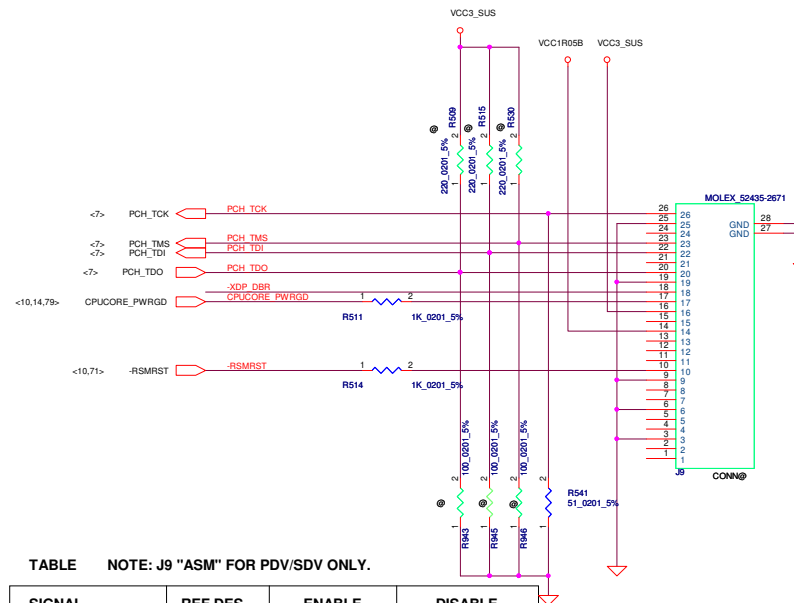
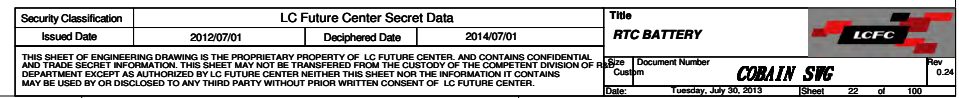
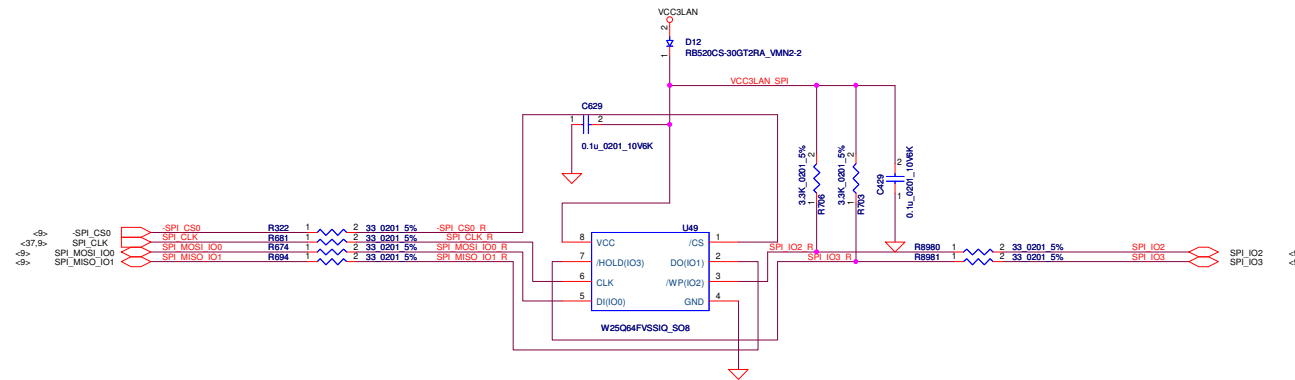


TABLE NOTE: J9 "ASM" FOR PDV/SDV ONLY.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R509 R943	220 100	NO ASM NO ASM
TMS	R530 R946	220 100	NO ASM NO ASM
TDI	R515 R945	220 100	NO ASM NO ASM
TCK	R541	51	51
CPUCORE_PWRGD	R511	ASM	NO ASM
-RSMRST	R514	ASM	NO ASM
	J9	ASM	NO ASM

↑  
LOGIC





TABLE


SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R681.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

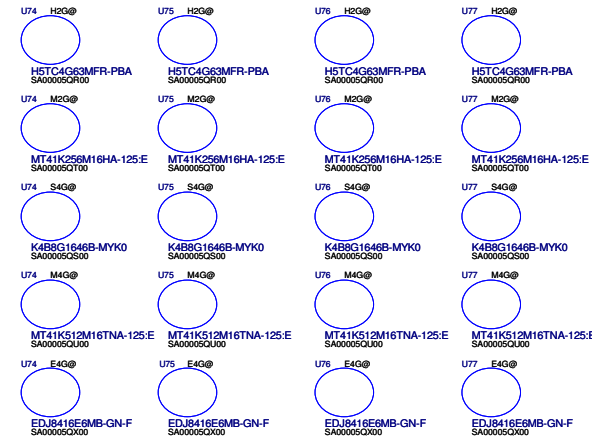
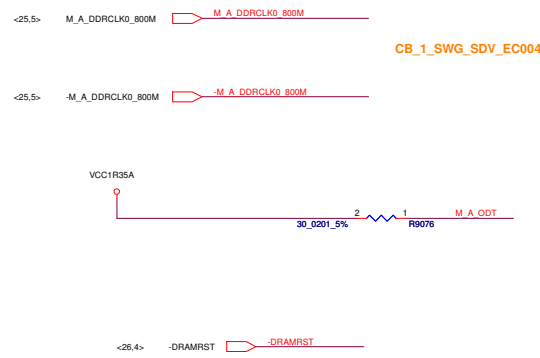
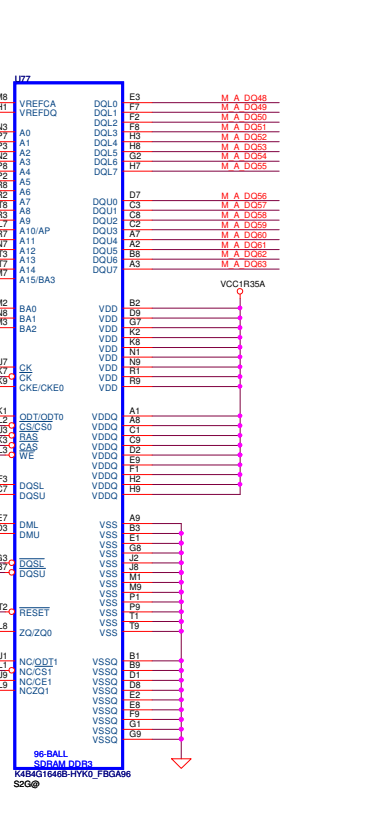
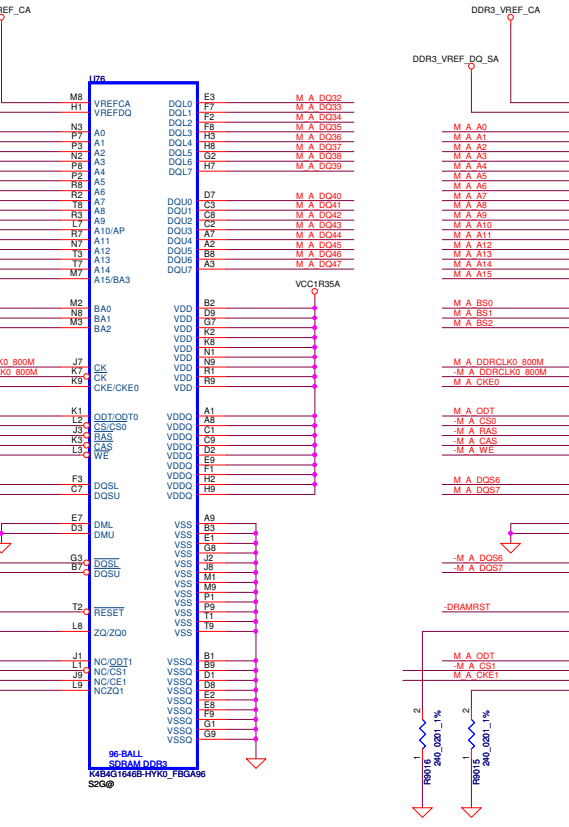
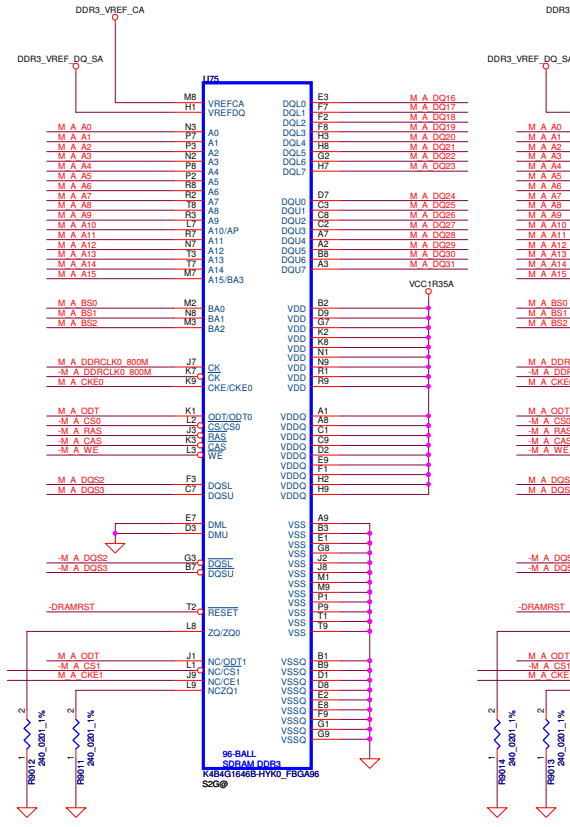
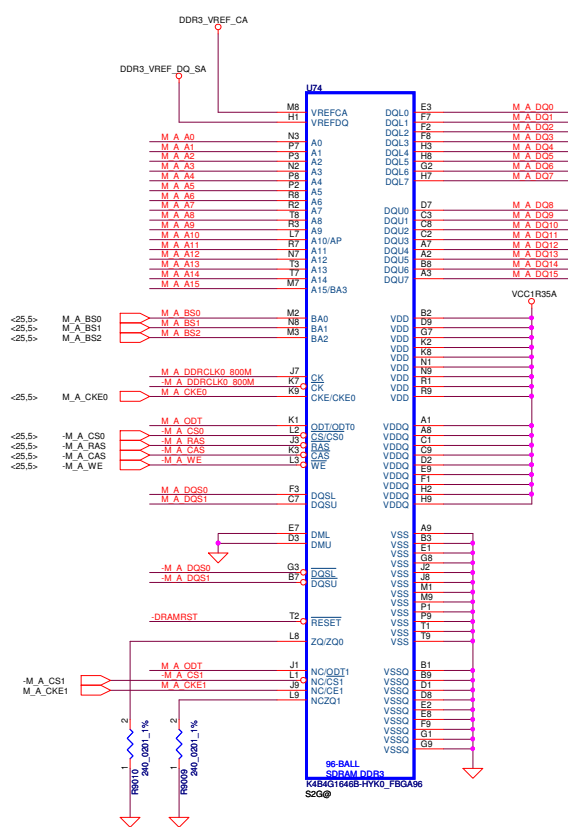
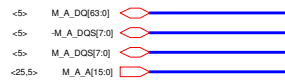
## U49 SPI ROM



vPro Model (16MB)		Non-vPro Model (8MB)	
WINBOND	W25Q128FVSIQ	WINBOND	W25Q64FVSSIQ
MACRONIX	MX25L12875FM2I-10G	MACRONIX	MX25L6475EM2I-10G
MICRON	N25Q128A13ESEC0F	MICRON	N25Q064A13ESEC0F

CB-1\_SWG\_SDV\_EC037

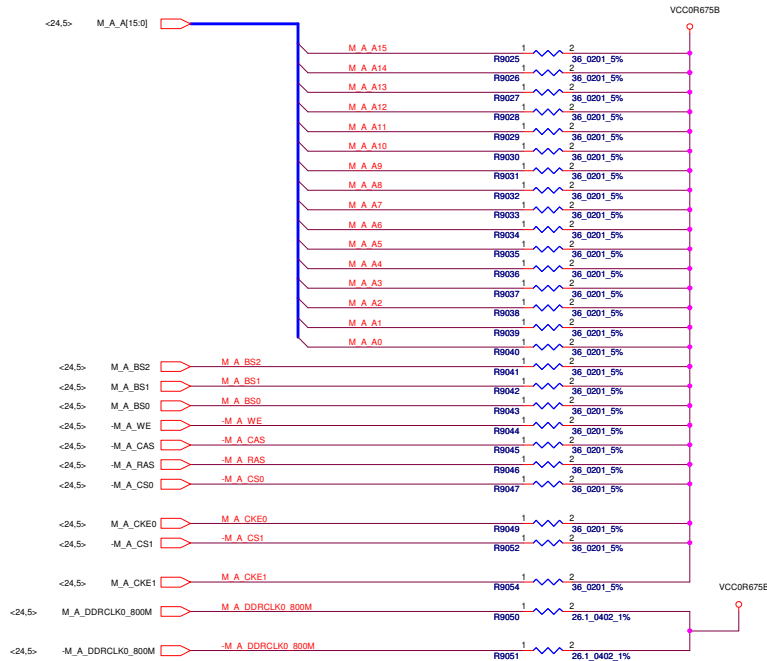
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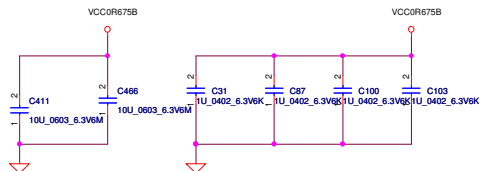


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<div> <div>Date</div> <div>Tuesday, July 30, 2013</div> <div>Sheet</div> <div>24</div> <div>of</div> <div>100</div> </div>						<div>Rev</div> <div>0.1</div>

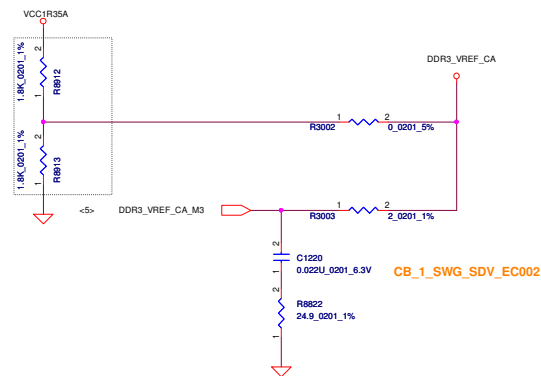
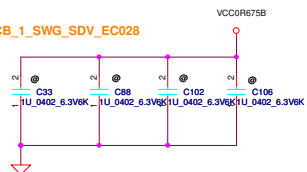




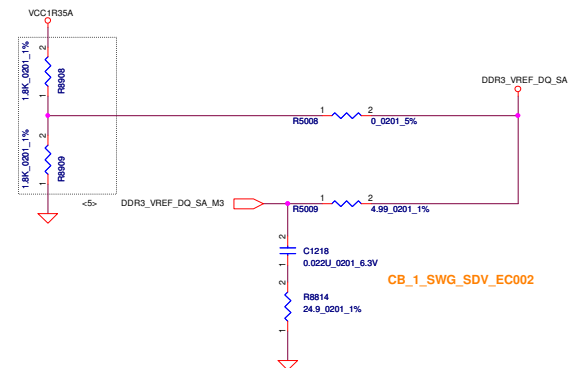
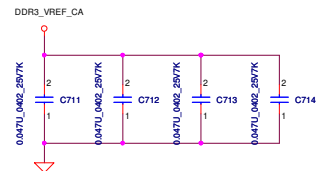
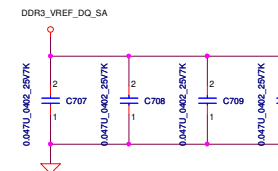
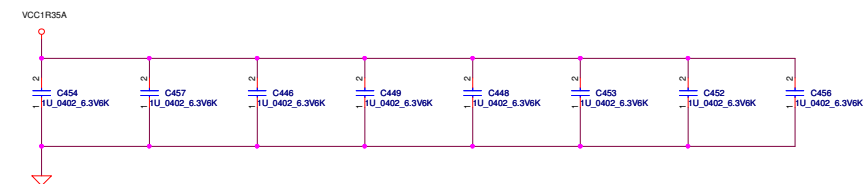
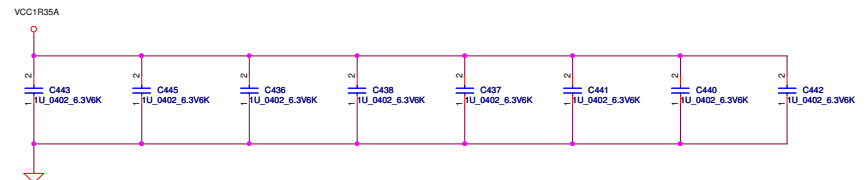
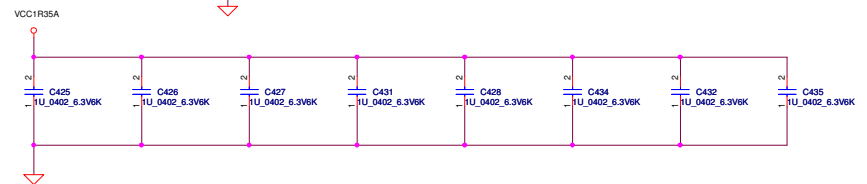
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CB\_1\_SWG\_SDV\_EC028

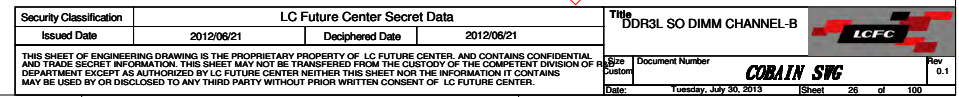



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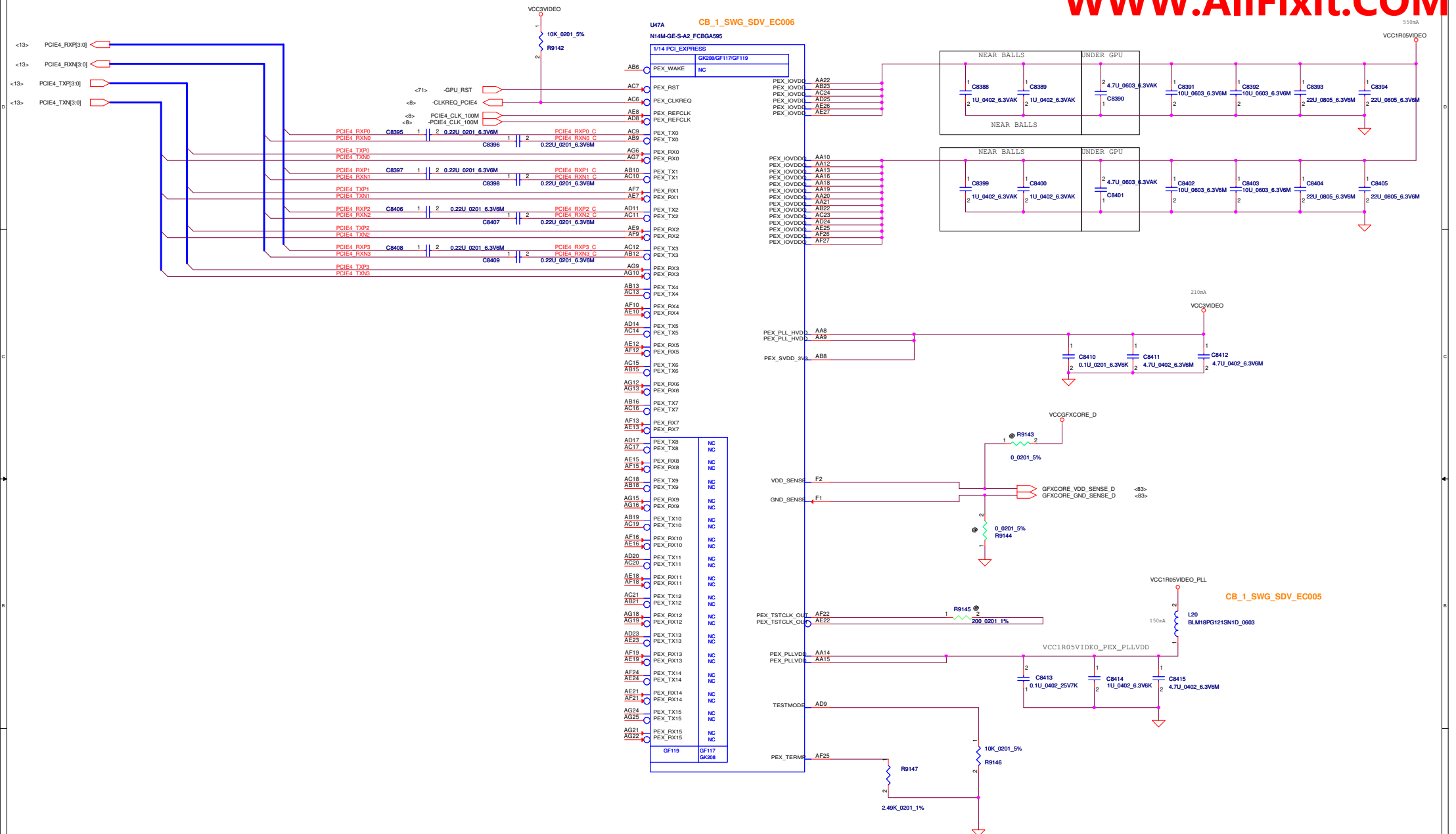


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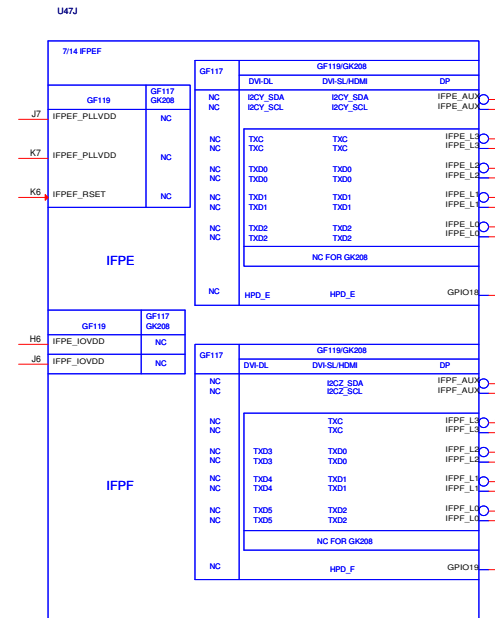
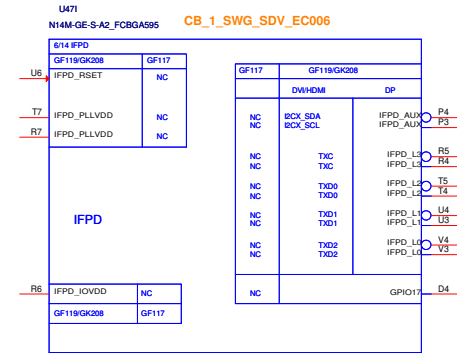
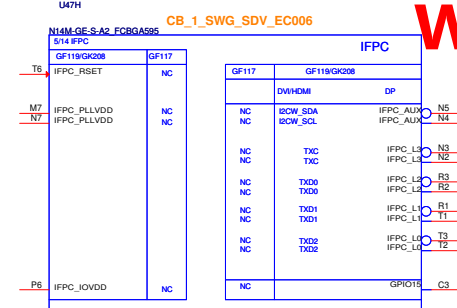
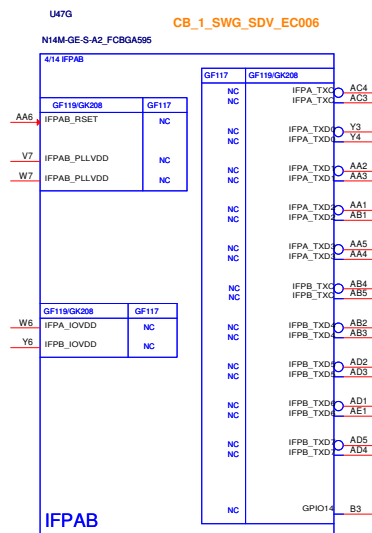


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				Date	Tuesday, July 30, 2013	Sheet	27 of 100



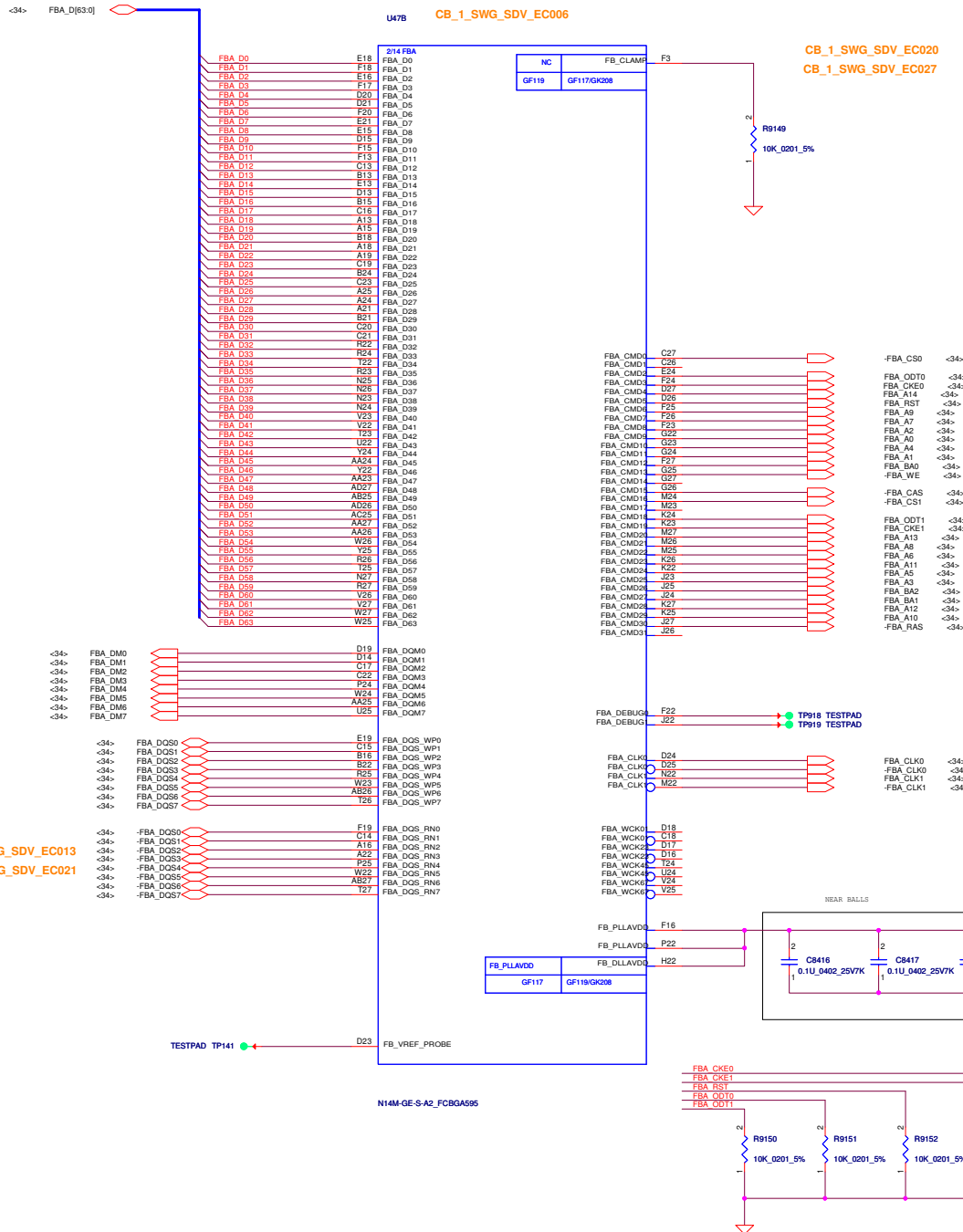
CB\_1\_SWG\_SDV\_EC006

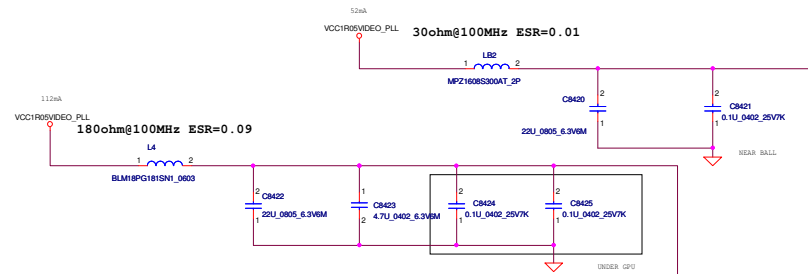
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Issued Date	2012/06/21	Deciphered Date	2012/06/21		N14M-GE(1/6) PEG I/F	
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CB\_1\_SWG\_SDV\_EC006

N14M-GE-S-A2\_FCBGA595





KDS	1ZZHAE27000CC0A
TXC	8Y27000005
EPSON	Q22FA1280007000

CB\_1\_SWG\_SDV\_EC019


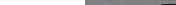


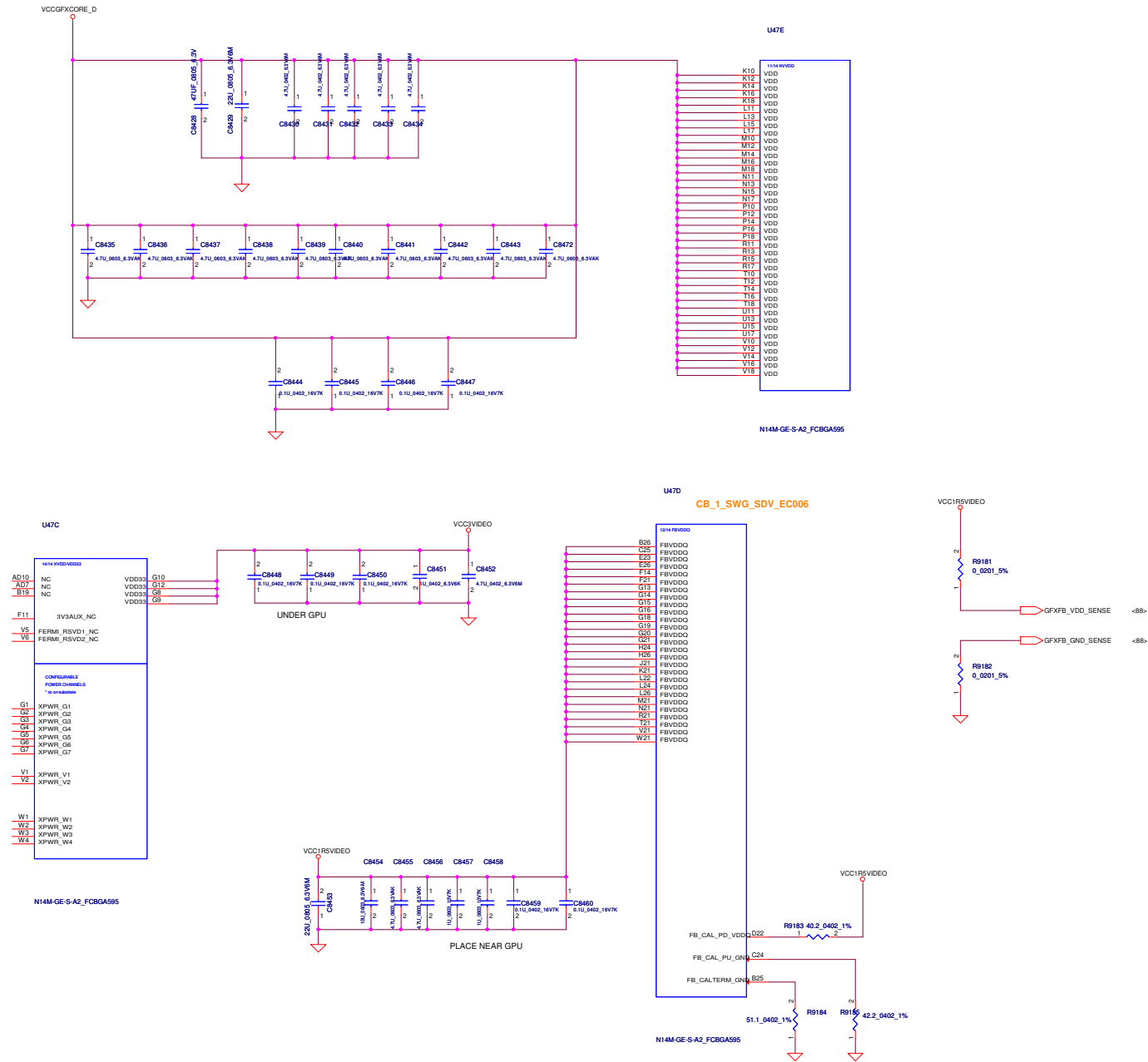
IF N14M-NE1/GE is used, change R9180 from 40.2K to NC

Micron 1GB(MT41J128M16JT-093G:K)							
STRAP 0		STRAP 1		STRAP 2		STRAP 3	
R9167	ASM	R9168	No ASM	R9169	No ASM	R9170	No ASM
R9175	No ASM	R9176	ASM	R9177	ASM	R9178	ASM

← LOGIC

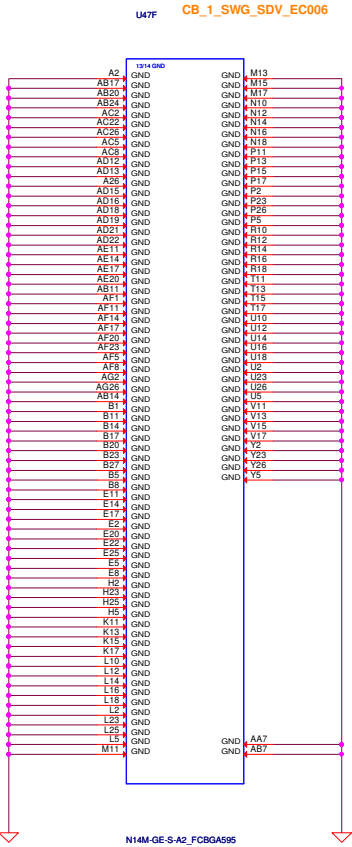
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Date	Tuesday, July 30, 2013		Sheet	31 of 100			




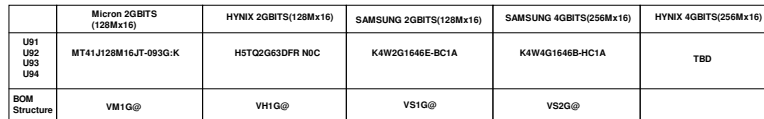
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CB\_1\_SWG\_SDV\_EC006

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						Size		Document Number	
Datum		8/26		Tuesday, July 30, 2013		Sheet		33 of 100	
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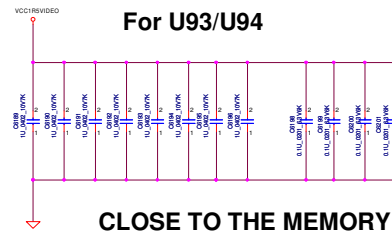
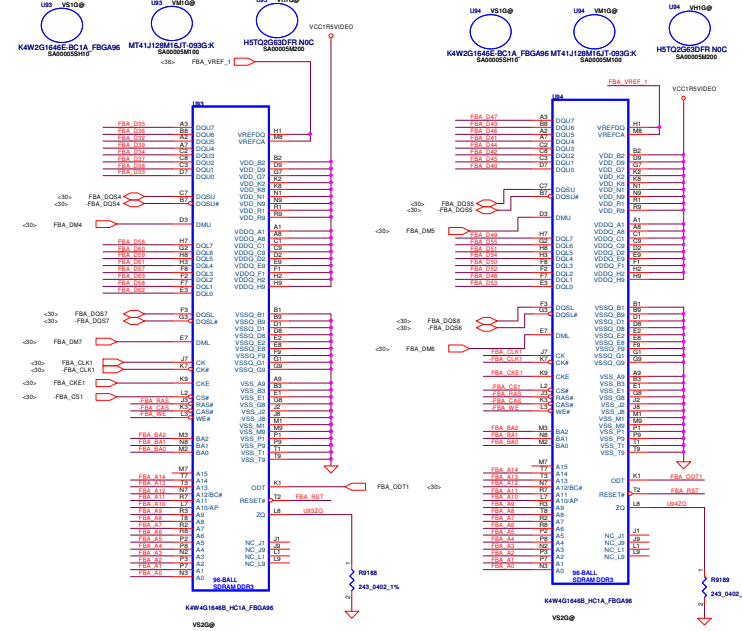


\*Notification\*

Sting-1 accepts 1GB support with DDR3. But Sting-1 has potential of 2GB support.

So we should check up 2GB(K4W4G1646B-HC1A) placement. K4W4G1646B-HC1A has largest X axis length (10mm) in VRAM.

MT41J128M6JT-093G:K has largest Y axis length (14mm). So estimation package size is most largest case (10mm \* 14mm).

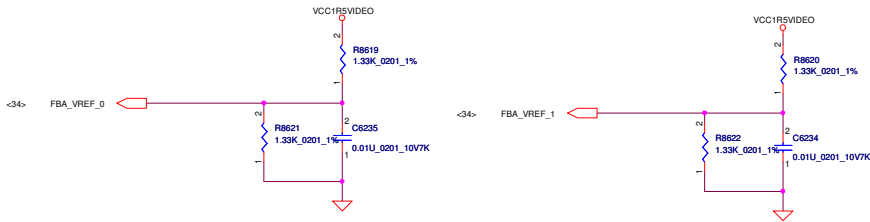



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				Sheet	35 of 100





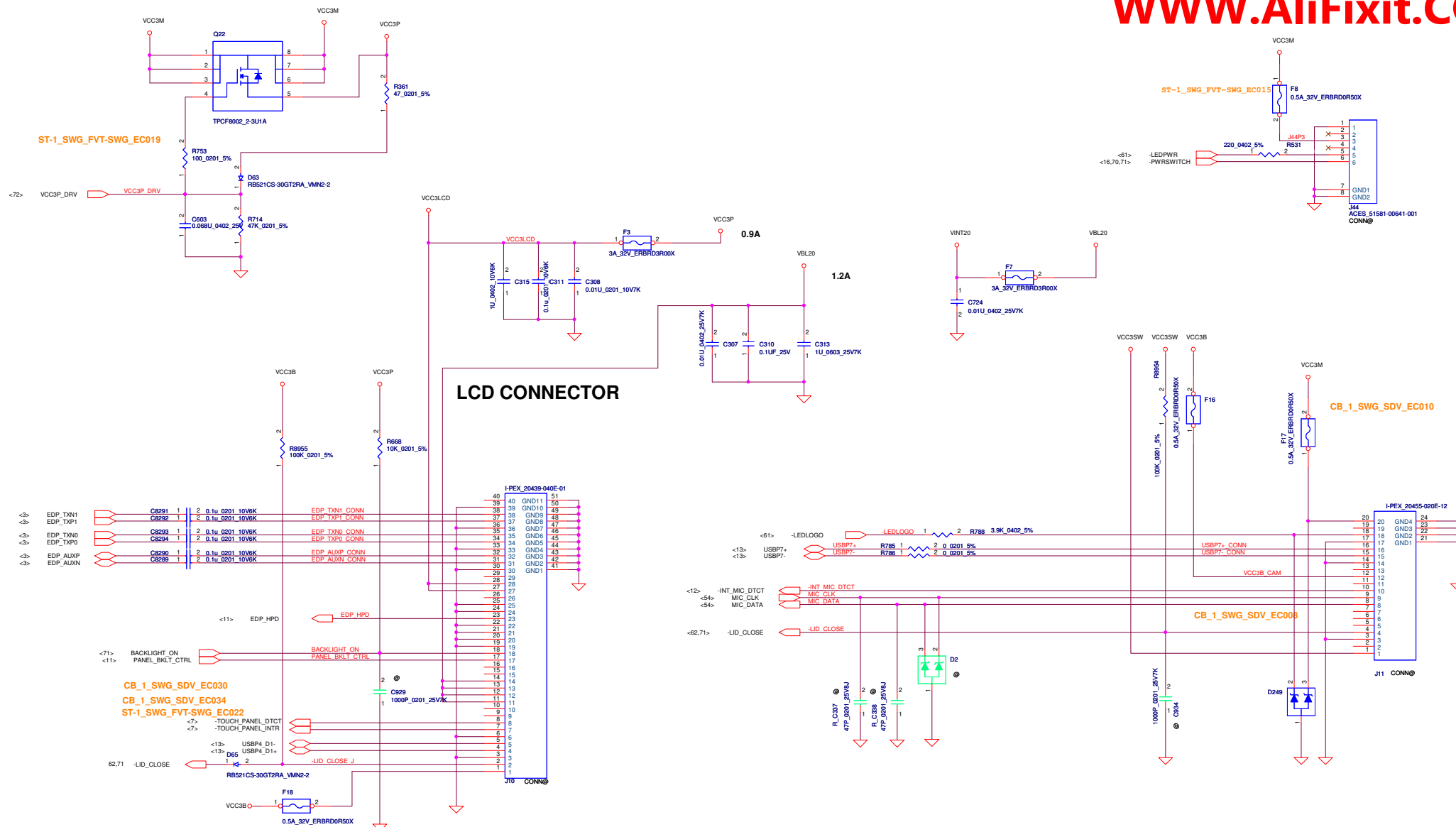
CORAIN SVG




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NEAR U58

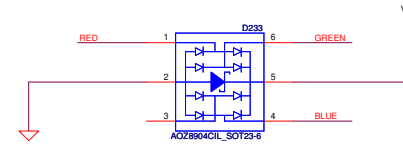
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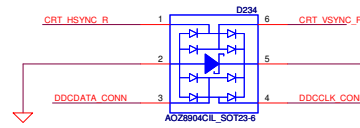
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				Sheet 38 of 100	

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				Date	Tuesday, July 30, 2013		



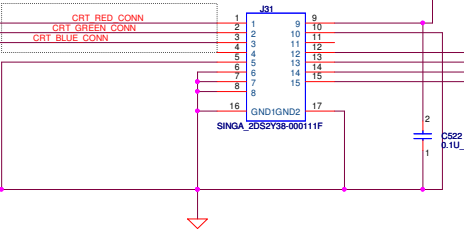
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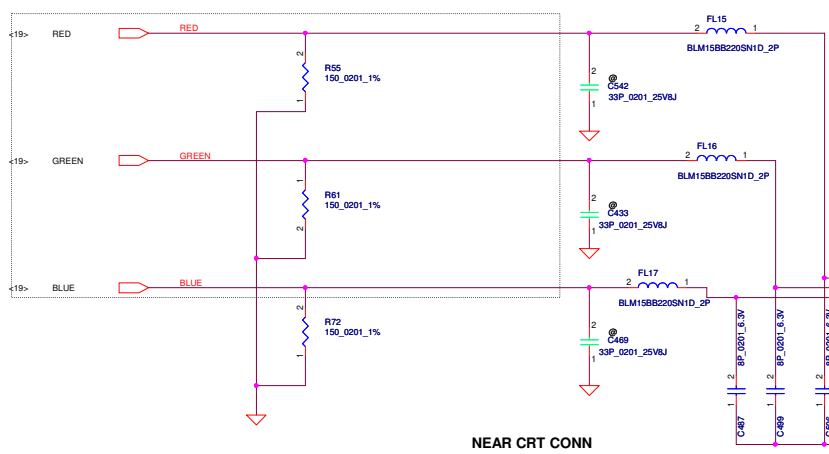
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CB\_1\_SWG\_SDV\_EC017

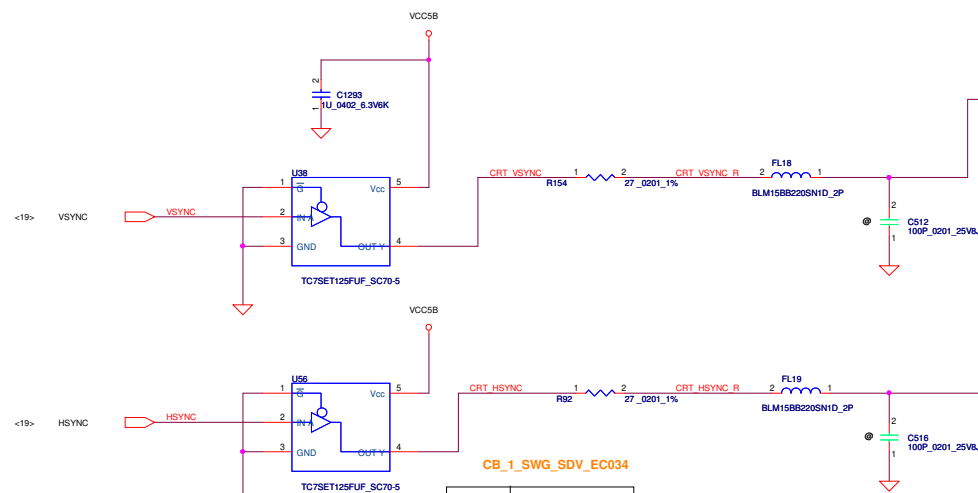
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500HM TRACE



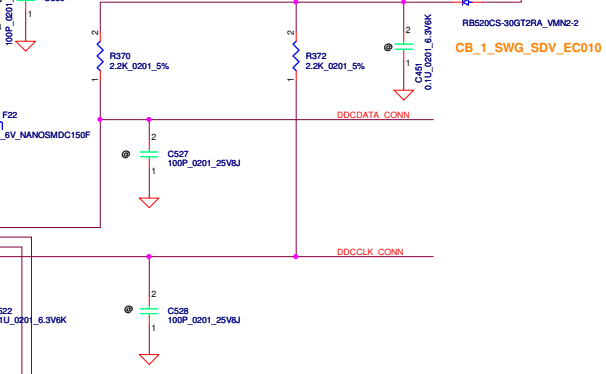
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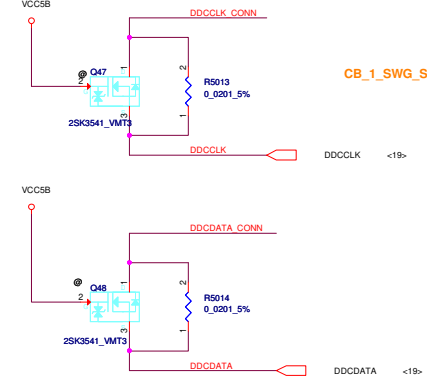
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Vender	P/N
TOSHIBA	TC7SET125FU
NXP	74AHCT1G125GW

CB\_1\_SWG\_SDV\_EC004




CB\_1\_SWG\_SDV\_EC004



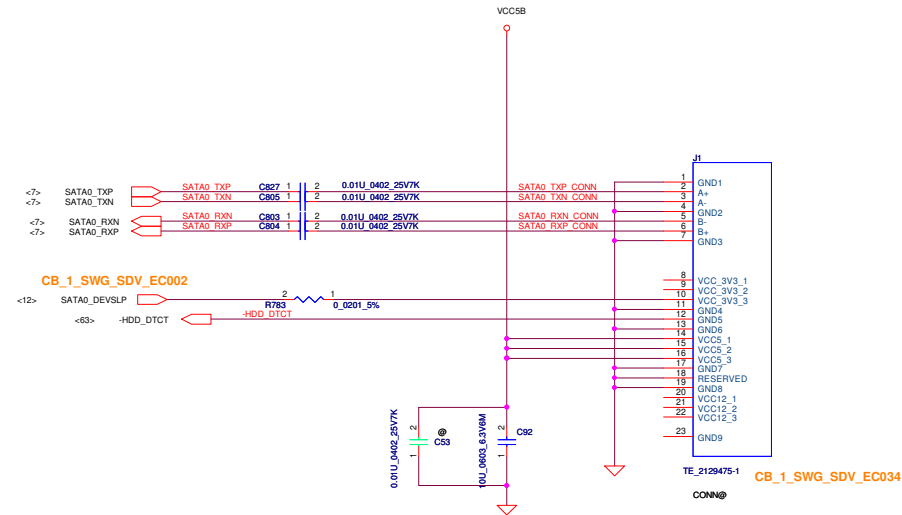





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Date	Tuesday, July 30, 2013		Sheet		43 of 100	

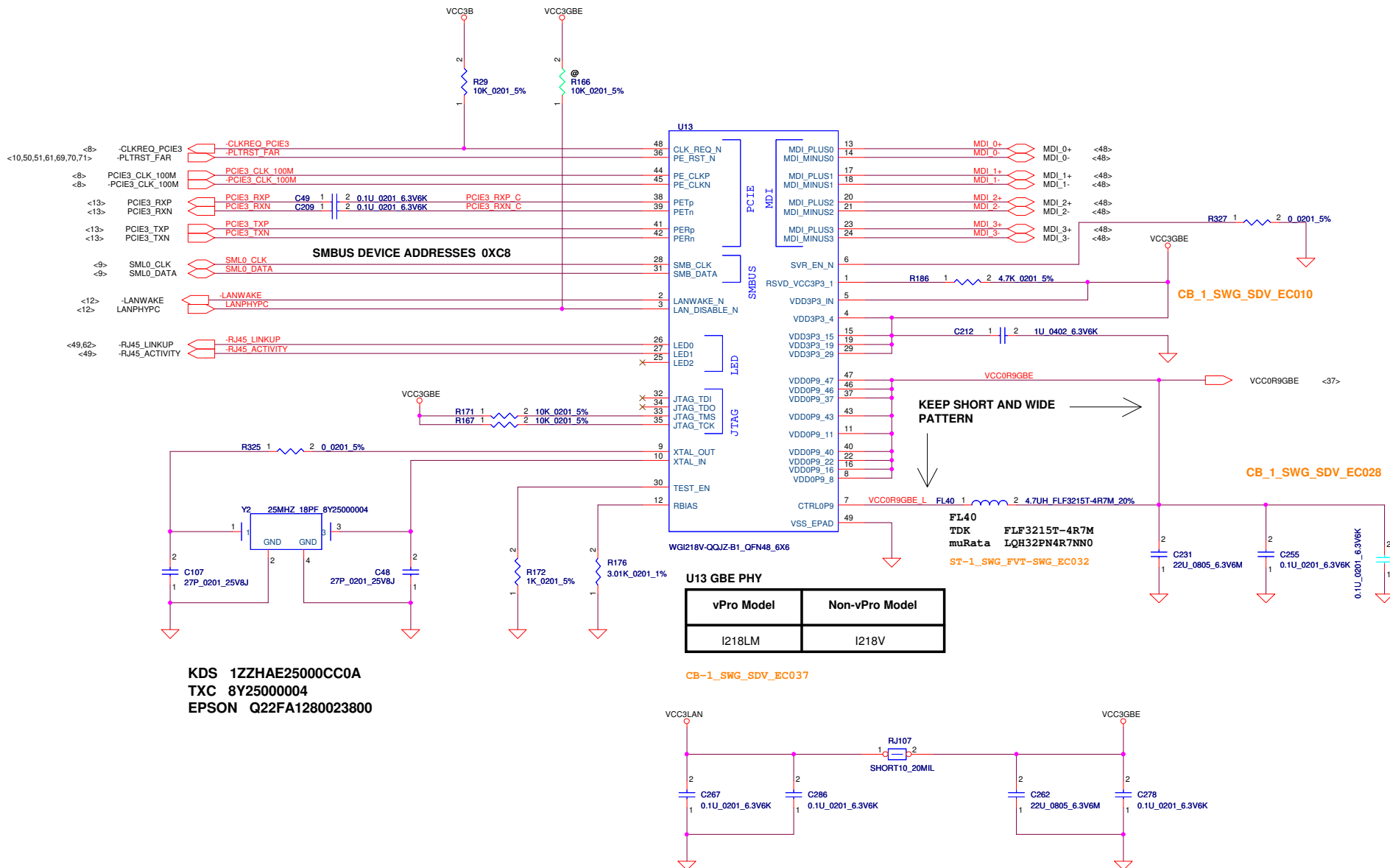
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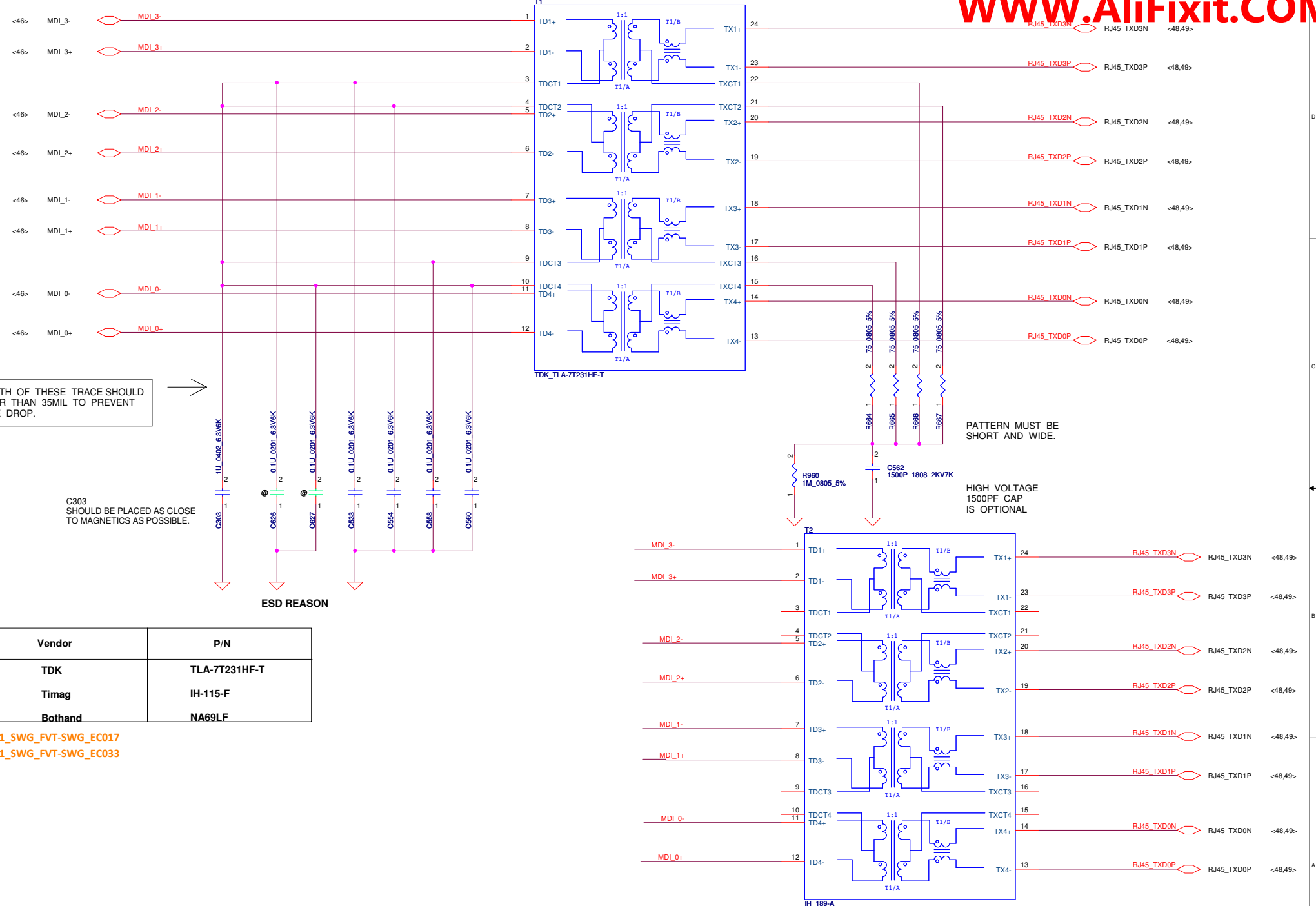


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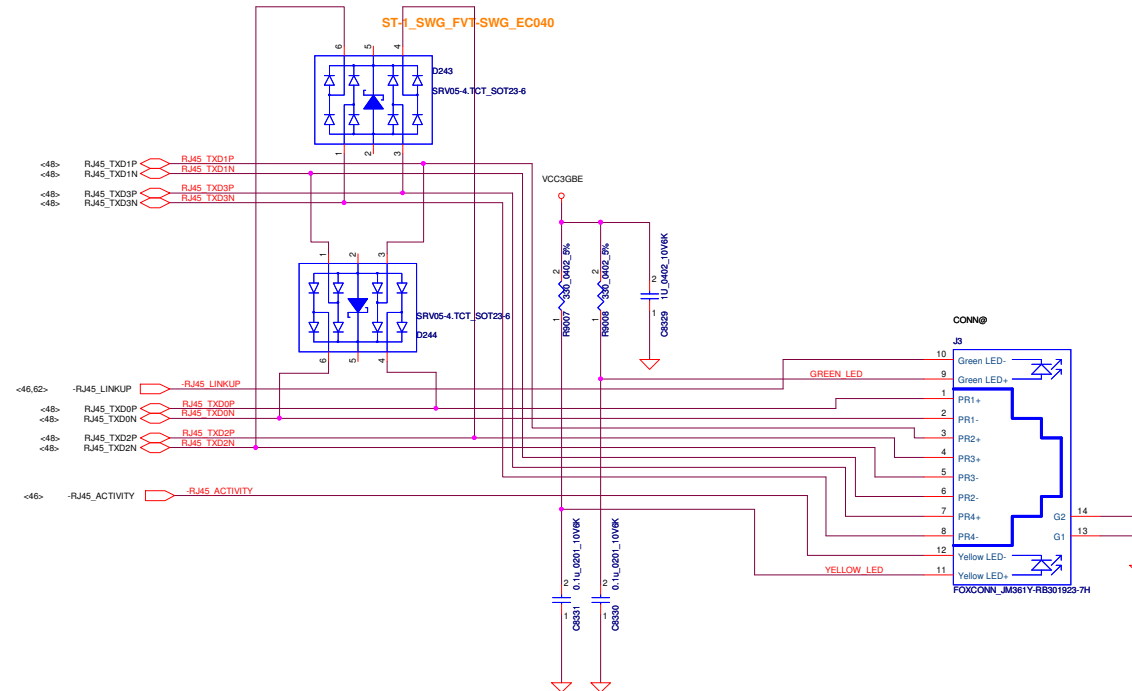
U13 GBE PHY	
vPro Model	Non-vPro Model
I218LM	I218V

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				Date:	Tuesday, July 30, 2013	Sheet	47 of 100



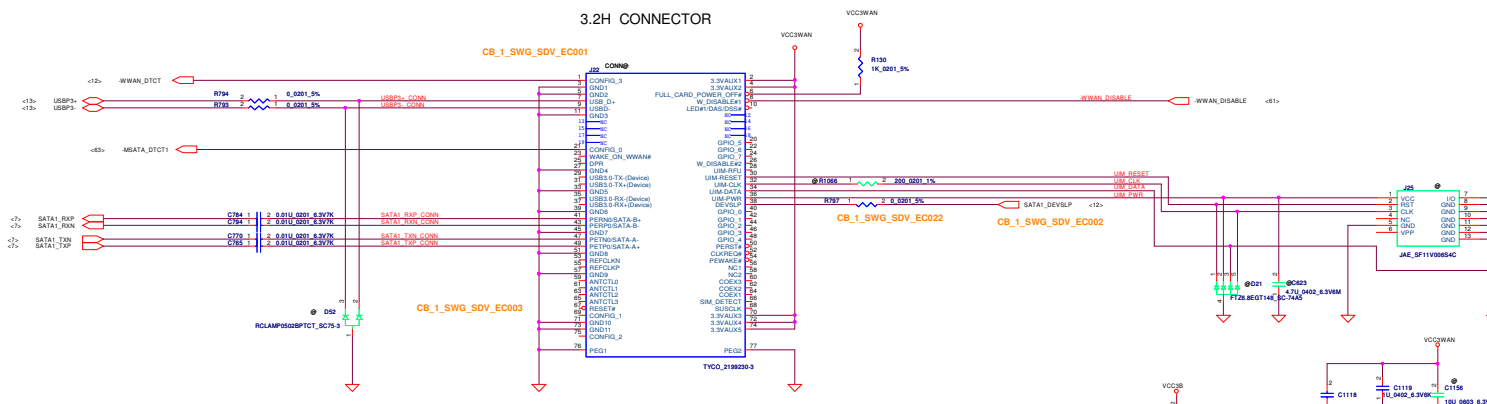




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Document Number	CORAIN SWG		Date: Tuesday, July 30, 2013
Sheet	49	of	100

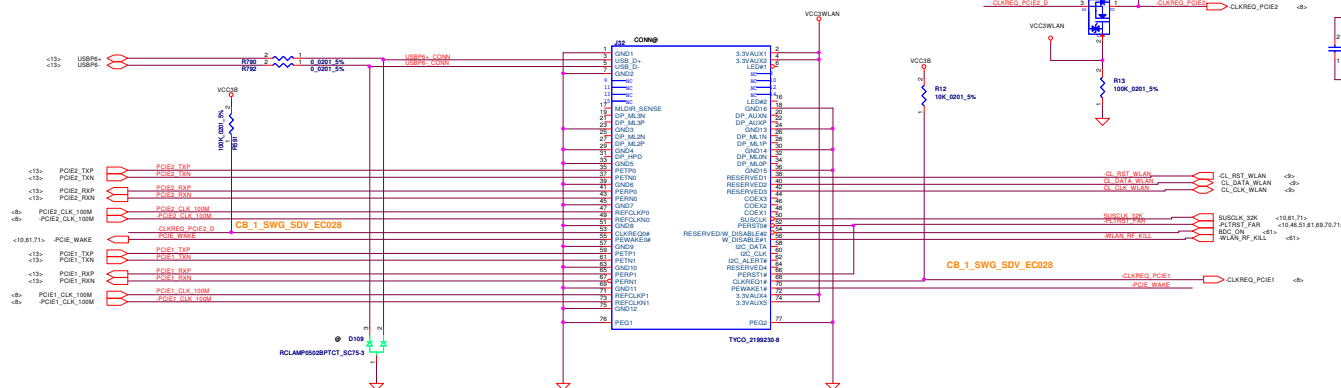
# TYPE-B NGFF CCARD FOR WWAN/SSD

3.2H CONNECTOR

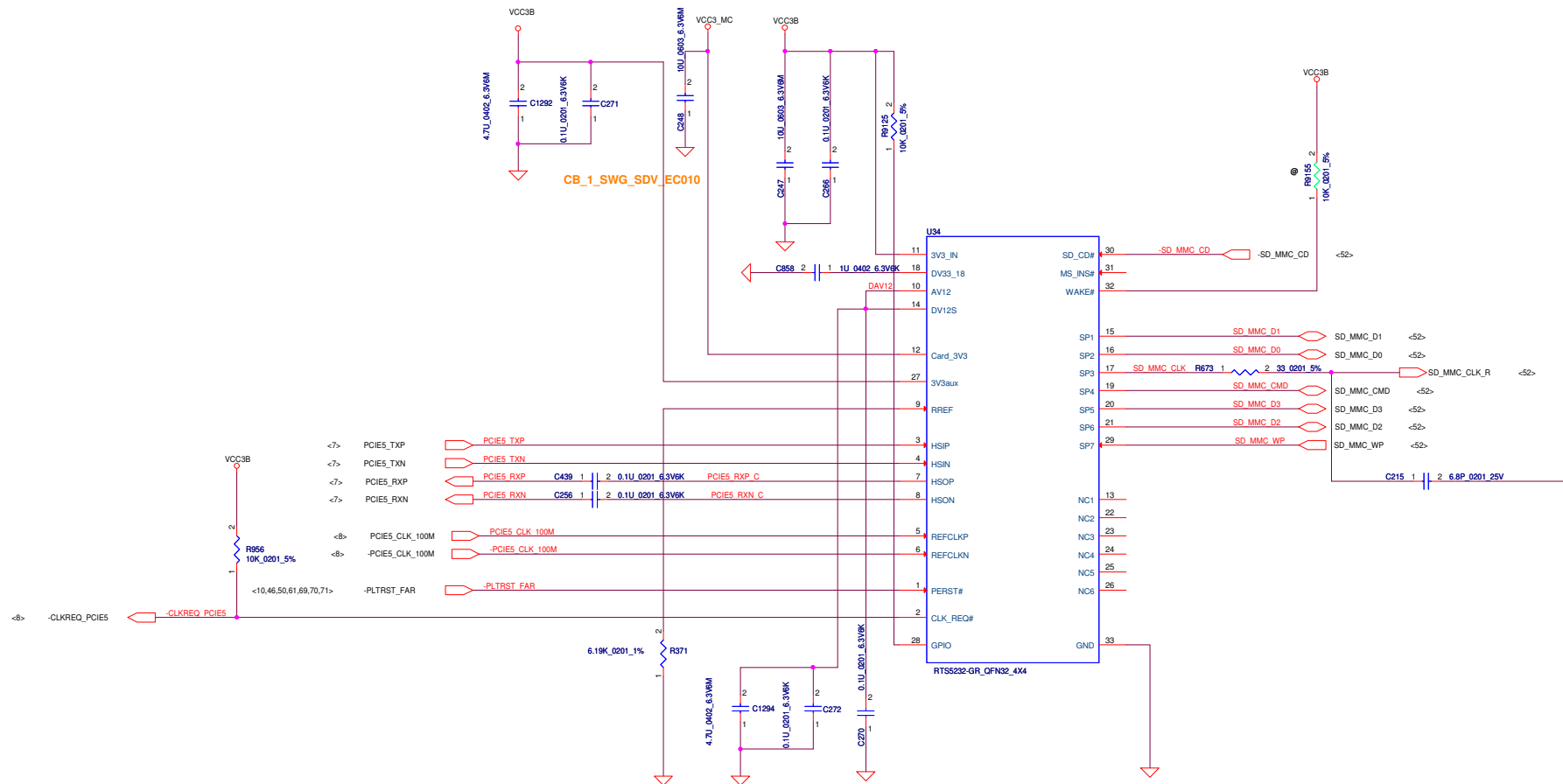


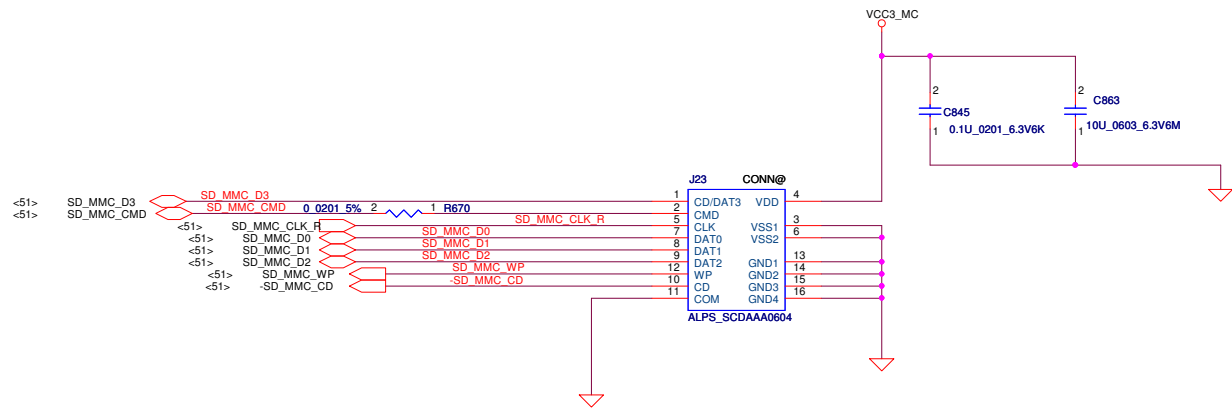
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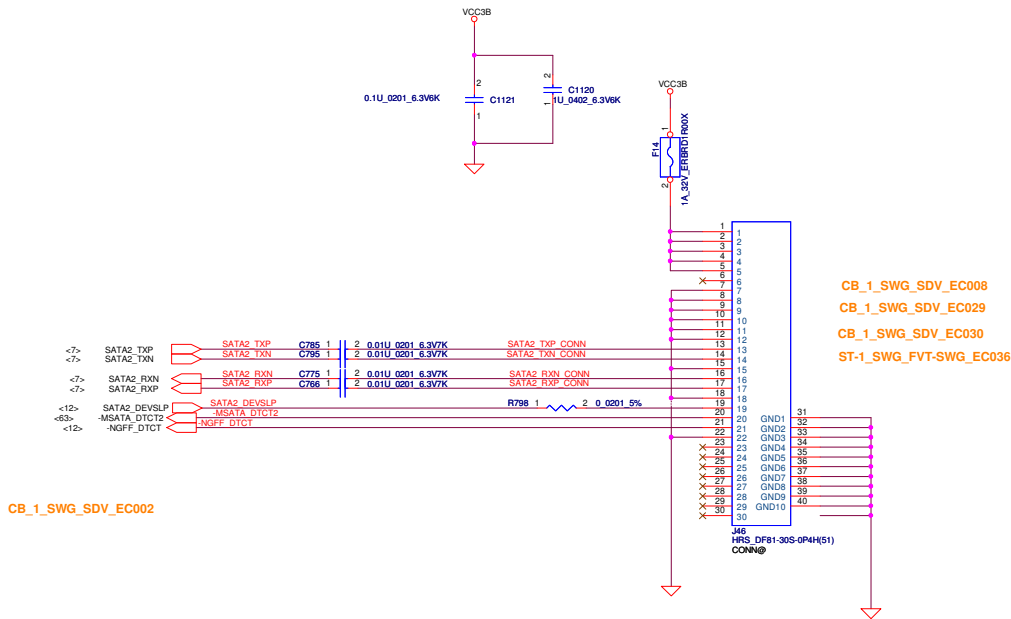
3.2H CONNECTOR



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Issued Date	2013/06/21	Discontinued Date	2013/06/21
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Doc	Document Number	COMAIN SW	
Rev	Version	Rev	Rev

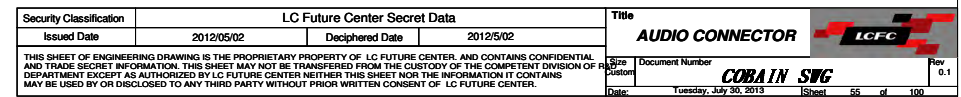


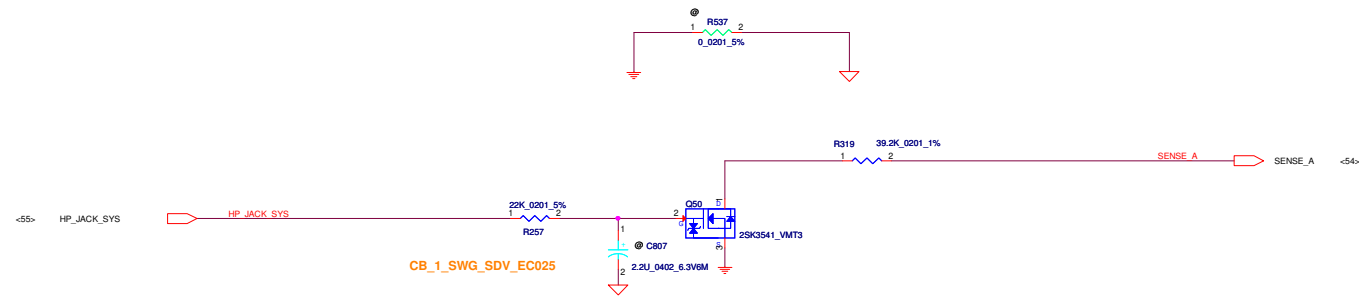




	Enable	Disable
R9097 R9015	NOASM ASM	ASM NOASM
R119	ASM	NOASM
L37 L38	ASM ASM	ASM ASM
R808 R809	NOASM NOASM	ASM ASM

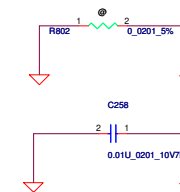
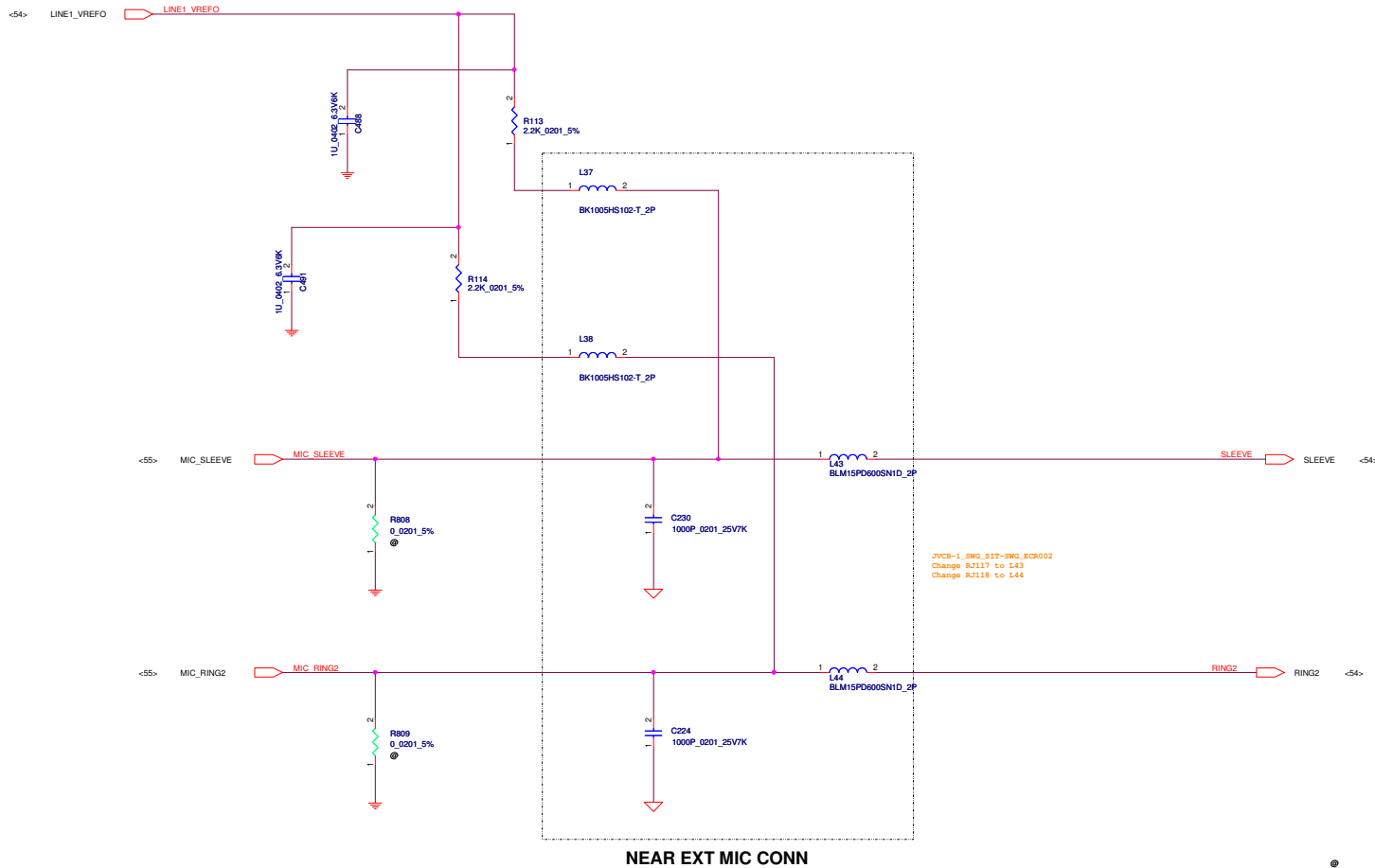






Security Classification	LC Future Center Secret Data		Title	AUDIO JACK SENSE	
Issued Date	2012/05/02	Deciphered Date	2012/5/02	Size	Document Number
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				Date:	Tuesday, July 30, 2013
				Sheet	58 of 100

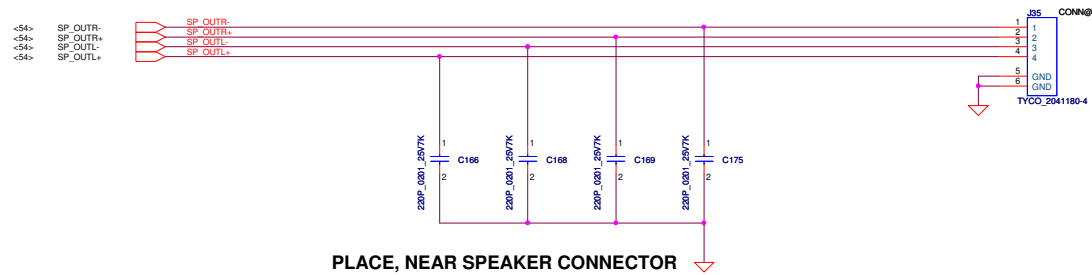




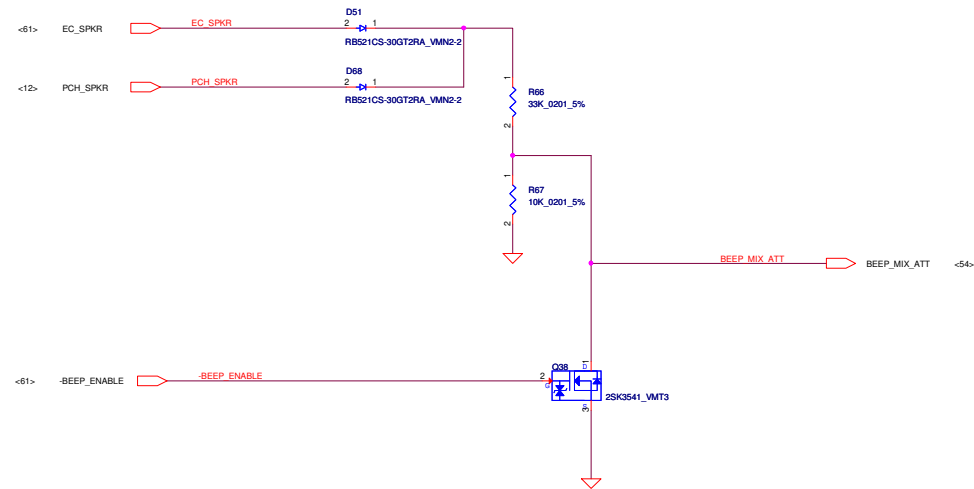
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COBAIN SFC




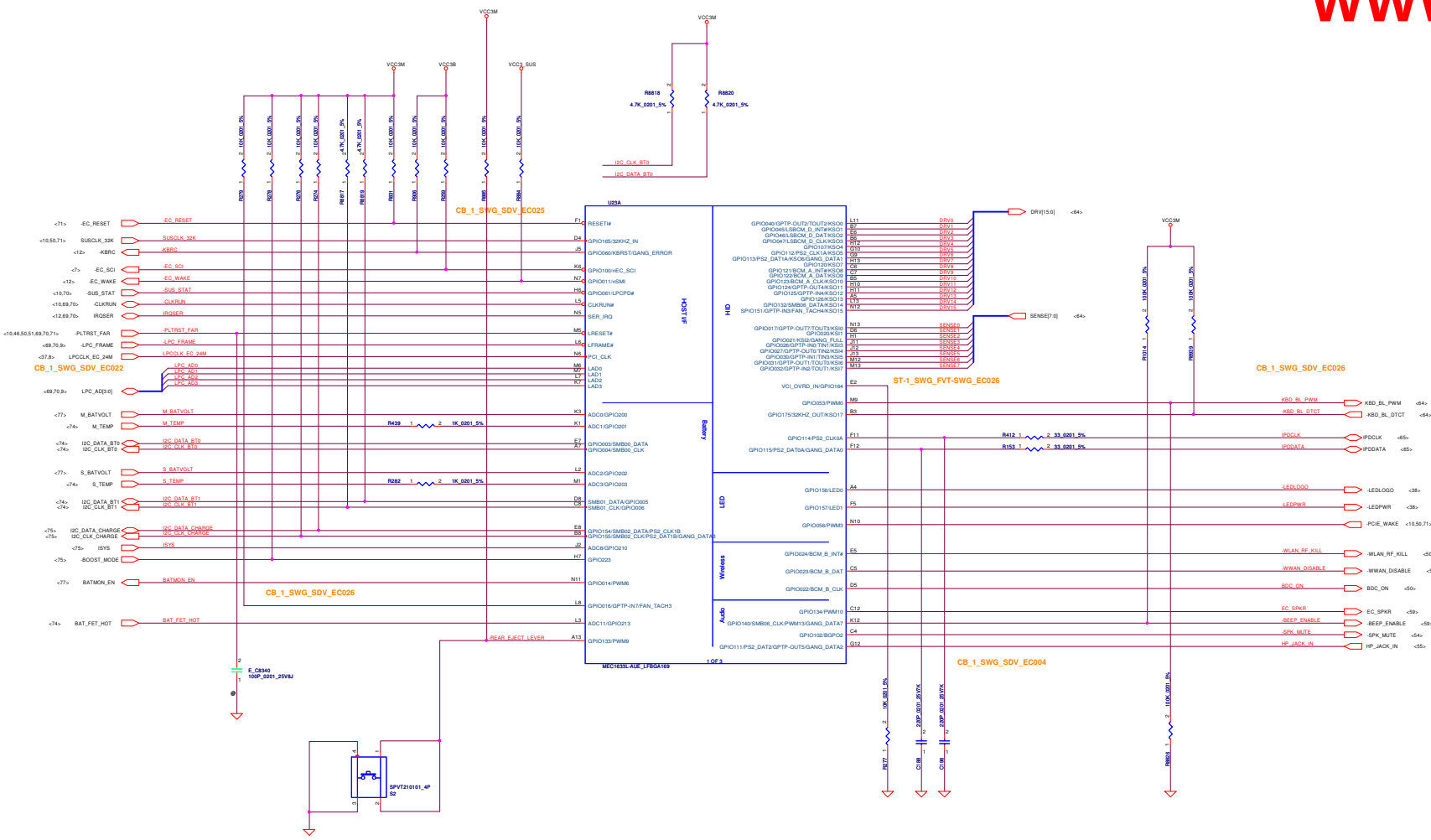
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Issued Date	2012/05/02	Deciphered Date	2012/5/02	Size	Document Number
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				Date:	Tuesday, July 30, 2013
				Sheet	58 of 100

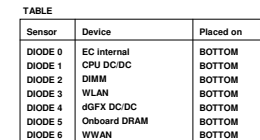


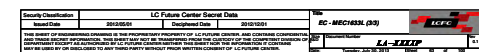
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Issued Date	2012/05/02	Deciphered Date	2012/5/02	Size	Document Number
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Date:	Tuesday, July 30, 2013	Sheet	59	of	100

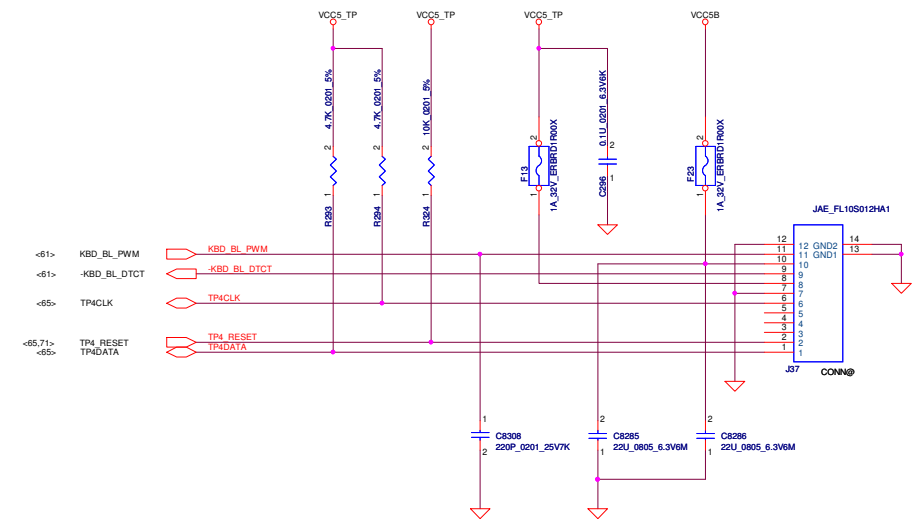
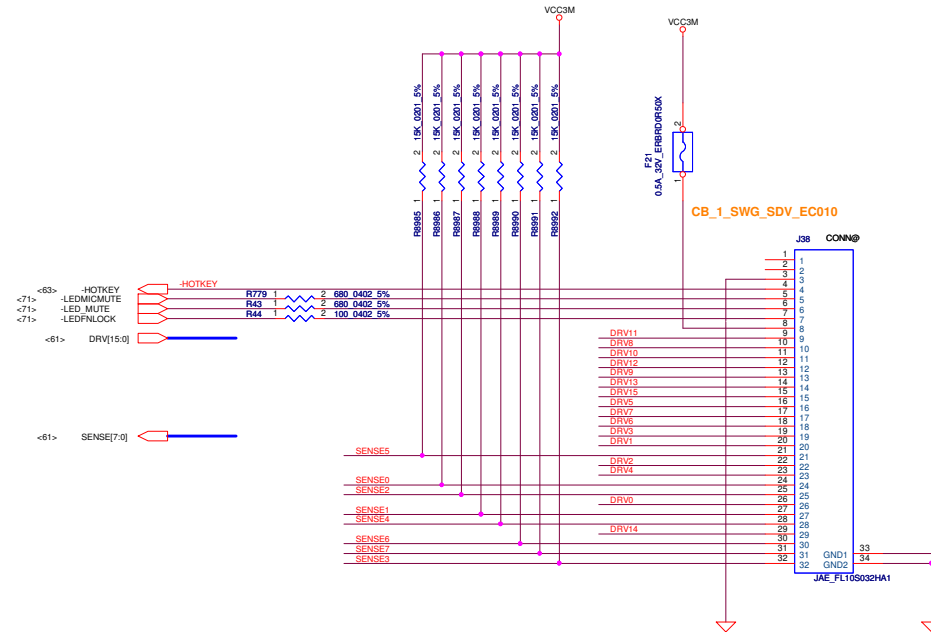
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				Document Number	CORAIN SVG	
				Date:	Tuesday, July 30, 2013	Sheet 60 of 100

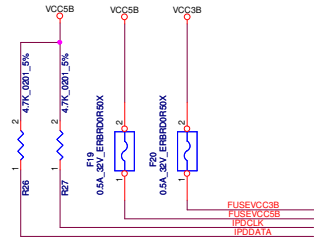




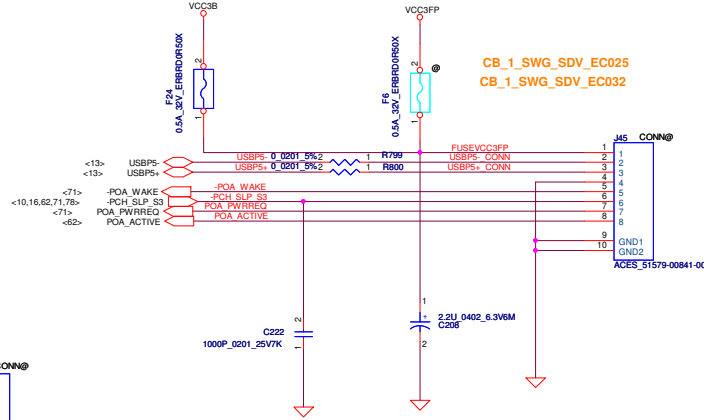
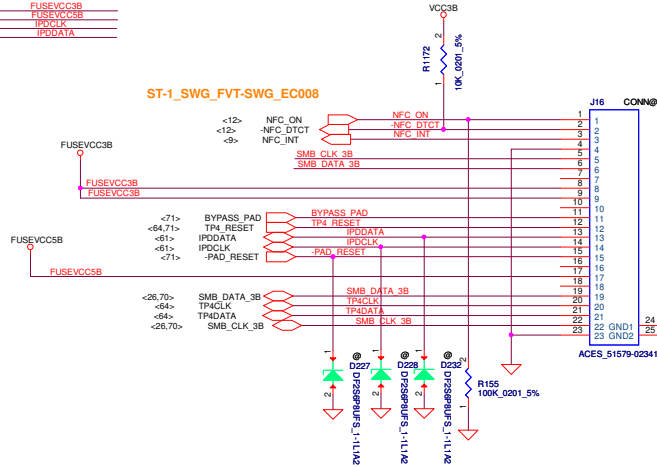






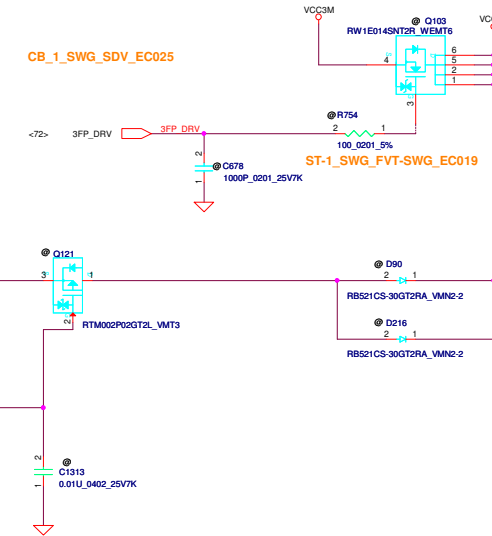


ST-1\_SWG\_FVT-SWG\_EC008

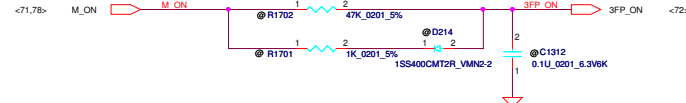


CB\_1\_SWG\_SDV\_EC025

ST-1\_SWG\_FVT-SWG\_EC019




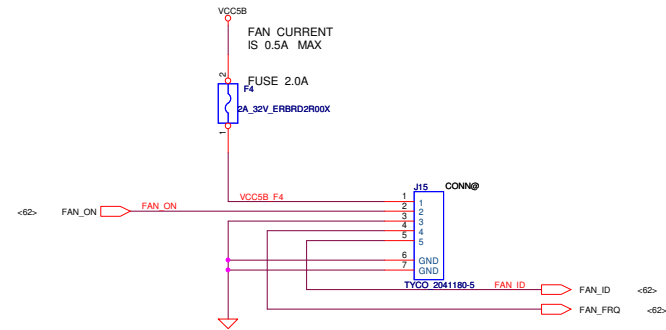
CB\_1\_SWG\_SDV\_EC025





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Issued Date	2012/06/21	Deciphered Date	2012/06/21	Document Number	C0BAIN SFC	
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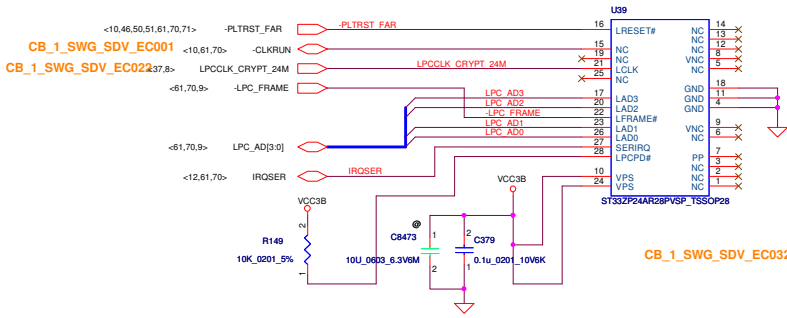
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				Document Number	Rev
				Date: Tuesday, July 30, 2013	0.1
				Sheet	66 of 100



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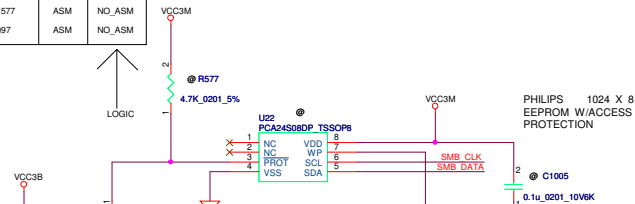
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Issued Date	2012/06/21	Deciphered Date	2012/06/21	G-SENSOR			
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				Date		0.1	
				Update	Tuesday, July 30, 2013	68 of 100	



TABLE

EEPROM	U22	U23
U22	ASM	NO_ASM
C1005	ASM	NO_ASM
R577	ASM	NO_ASM
Q97	ASM	NO_ASM

LOGIC



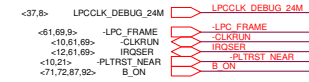
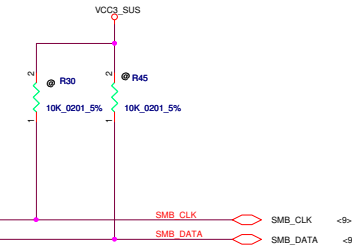
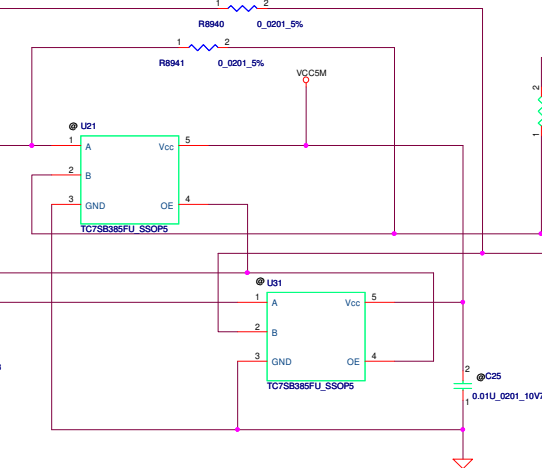
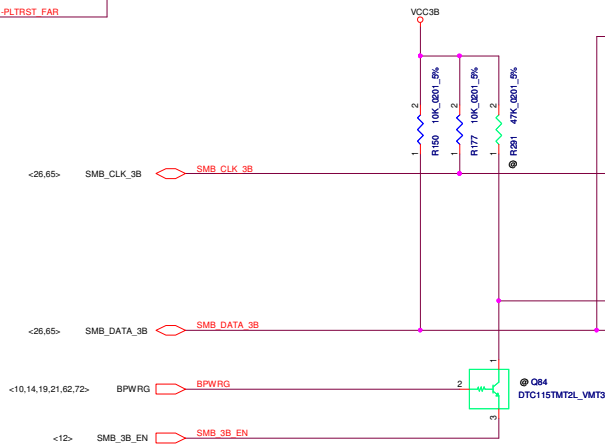
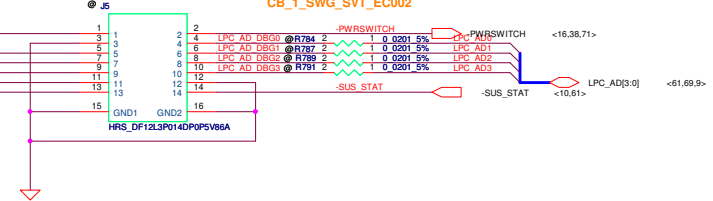
ST-1\_SWG\_SDV\_EC132

TABLE

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	J5	ASM	NO_ASM
	R220	ASM	NO_ASM

LOGIC


CB\_1\_SWG\_SDV\_EC022

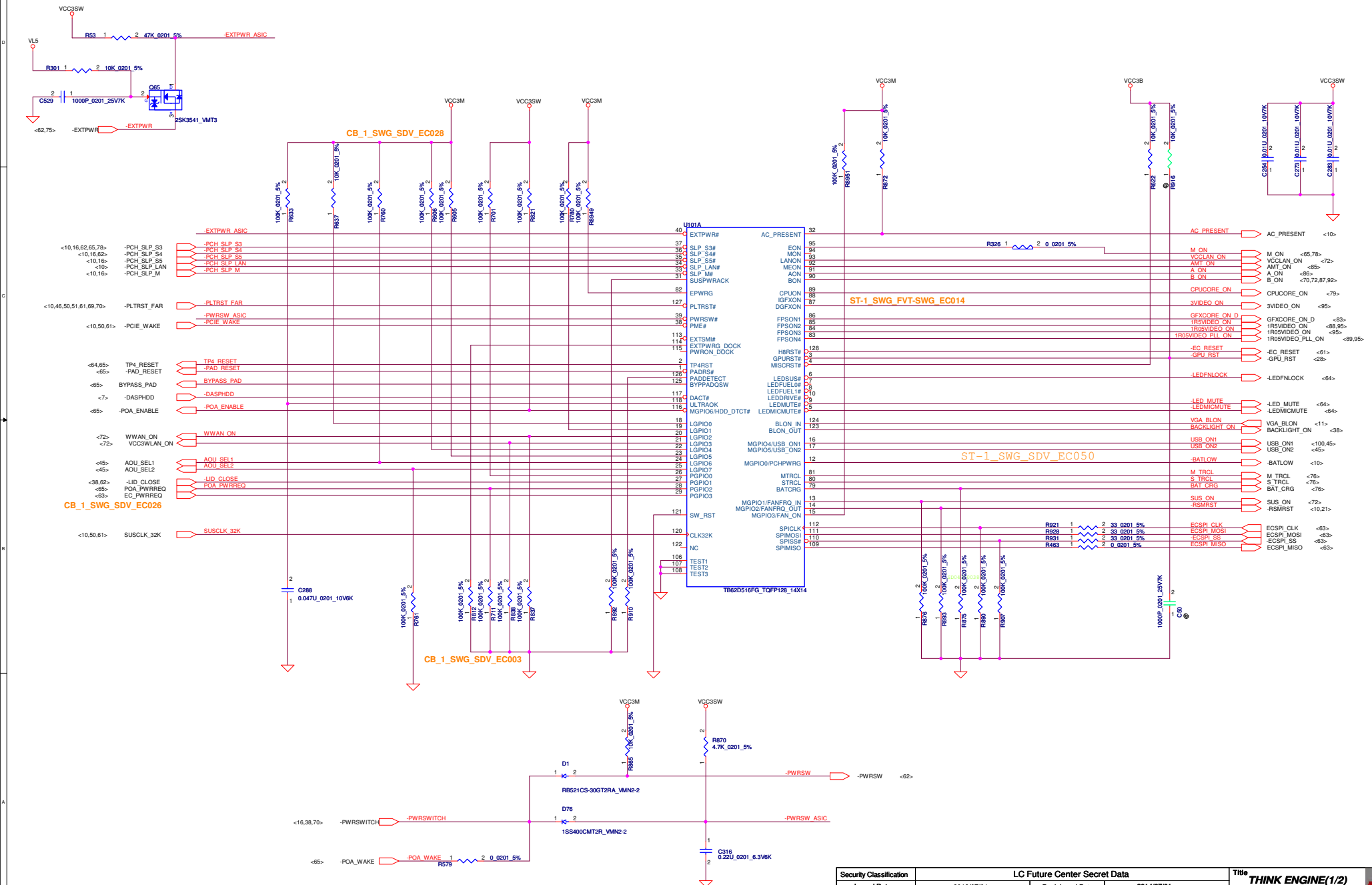
CB\_1\_SWG\_SDV\_EC028  
CB\_1\_SWG\_SVT\_EC002



TABLE

EEPROM	U22	U23
U21	ASM	NO_ASM
U31	ASM	NO_ASM
C25	ASM	NO_ASM
R291	ASM	NO_ASM
Q84	ASM	NO_ASM
R8941	NO_ASM	ASM
R8940	NO_ASM	ASM
R30	ASM	NO_ASM
R45	ASM	NO_ASM

LOGIC

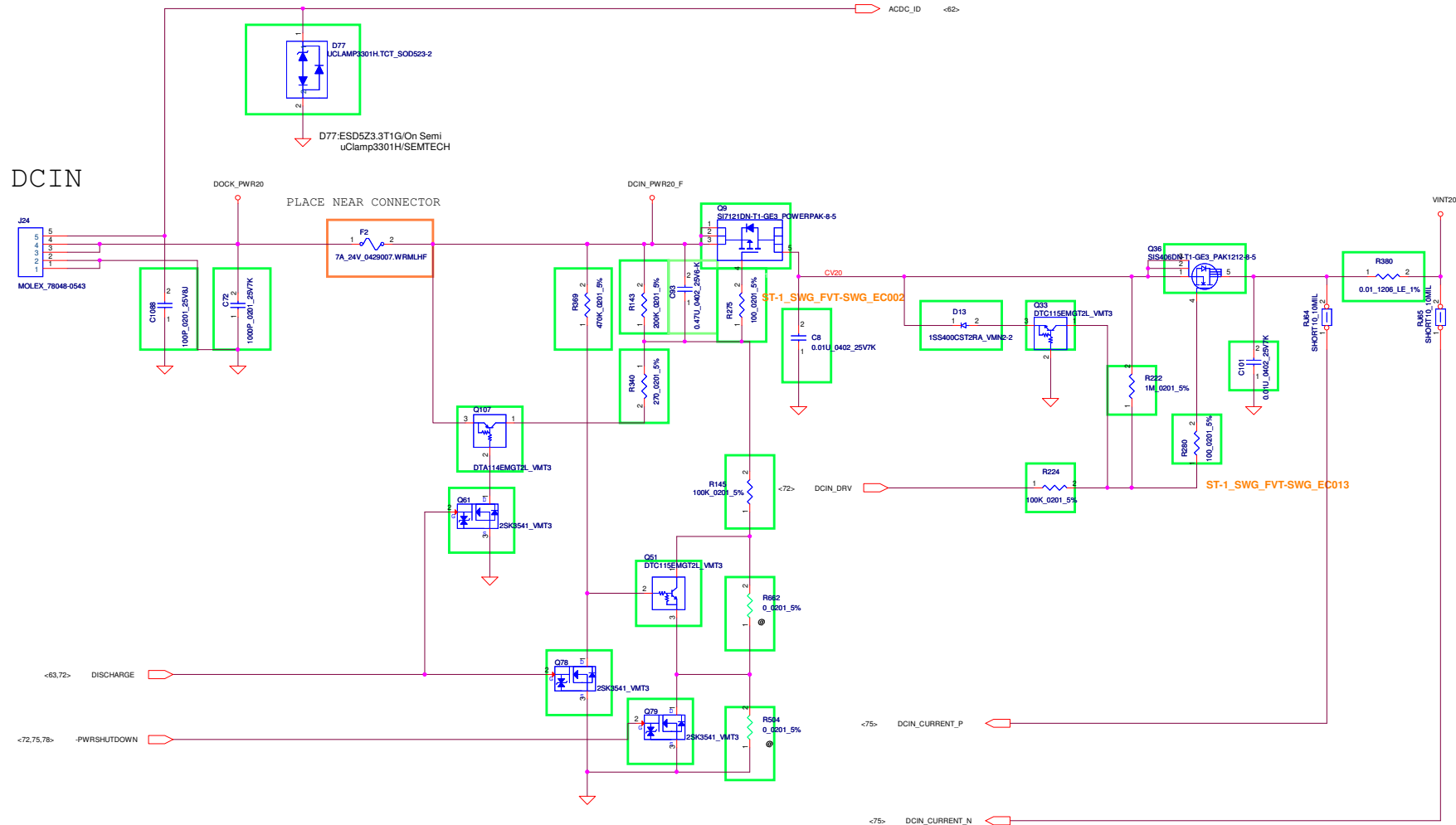
Security Classification	LC Future Center Secret Data		Title	EEPROM/SMBUS SW		
Issued Date	2012/05/02	Deciphered Date	2012/05/02			
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Date:	Tuesday, July 30, 2013	Sheet	70	of	100	



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Issued Date	2018/07/01	Deciphered Date	2014/07/01	THINK ENGINE(1/2)			
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				Date	Tuesday, July 30, 2013	Sheet	71 of 100



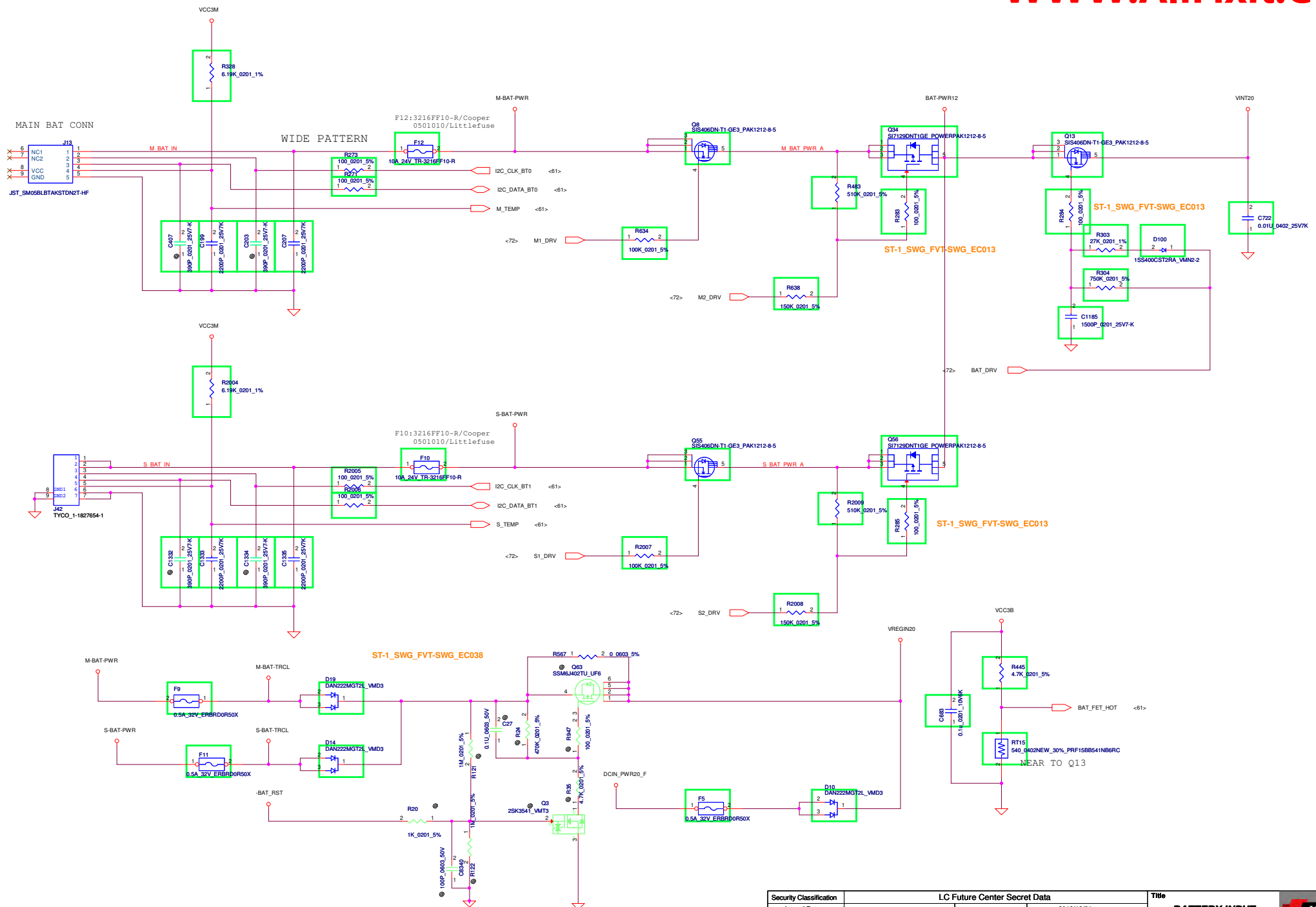





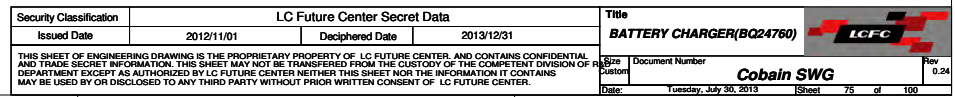
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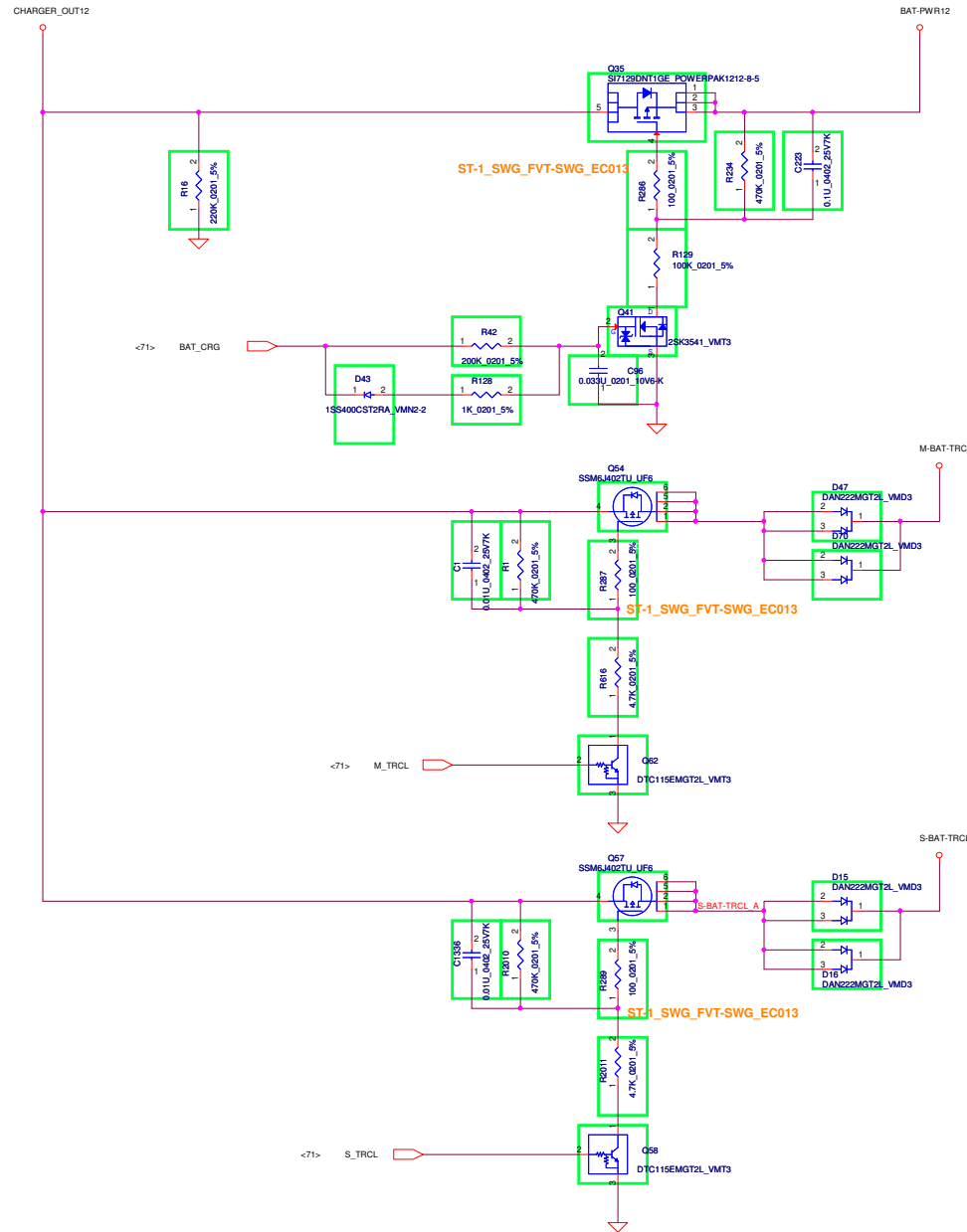
PEAK SHIFT	YES	NO
R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
Q51	ASM	NO-ASM

LOGIC

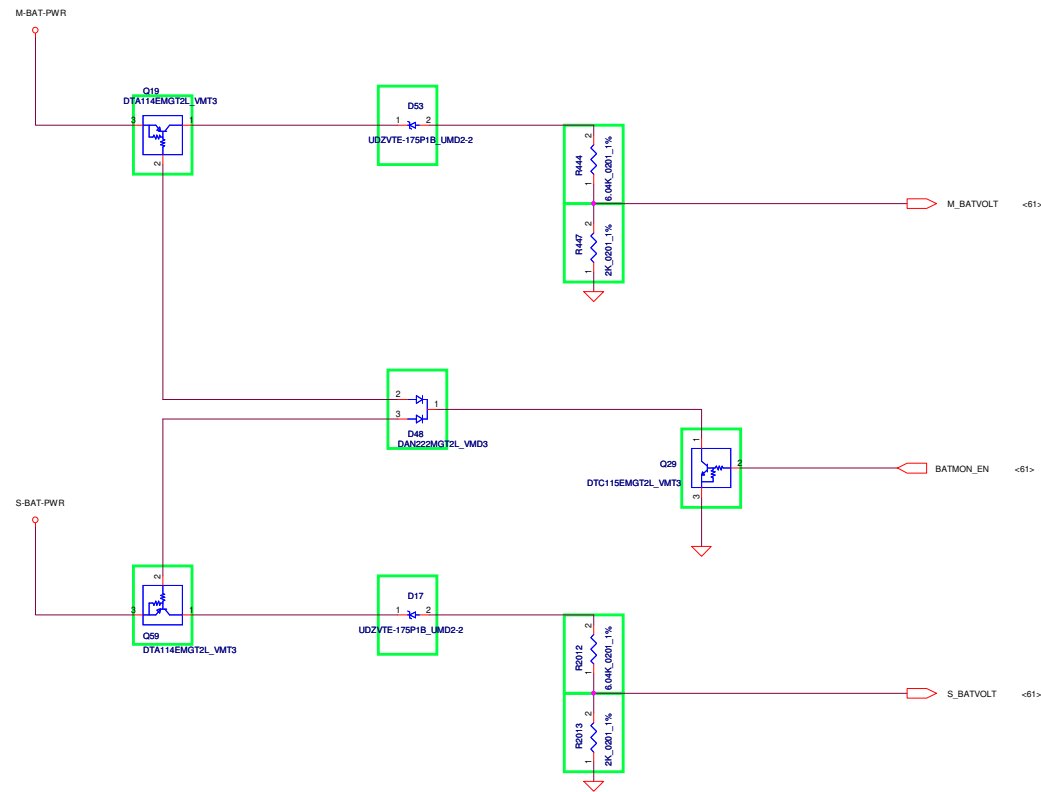



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				Date	Tuesday, July 30, 2013	Sheet	74 of 100
				Cobain SWG			0.24





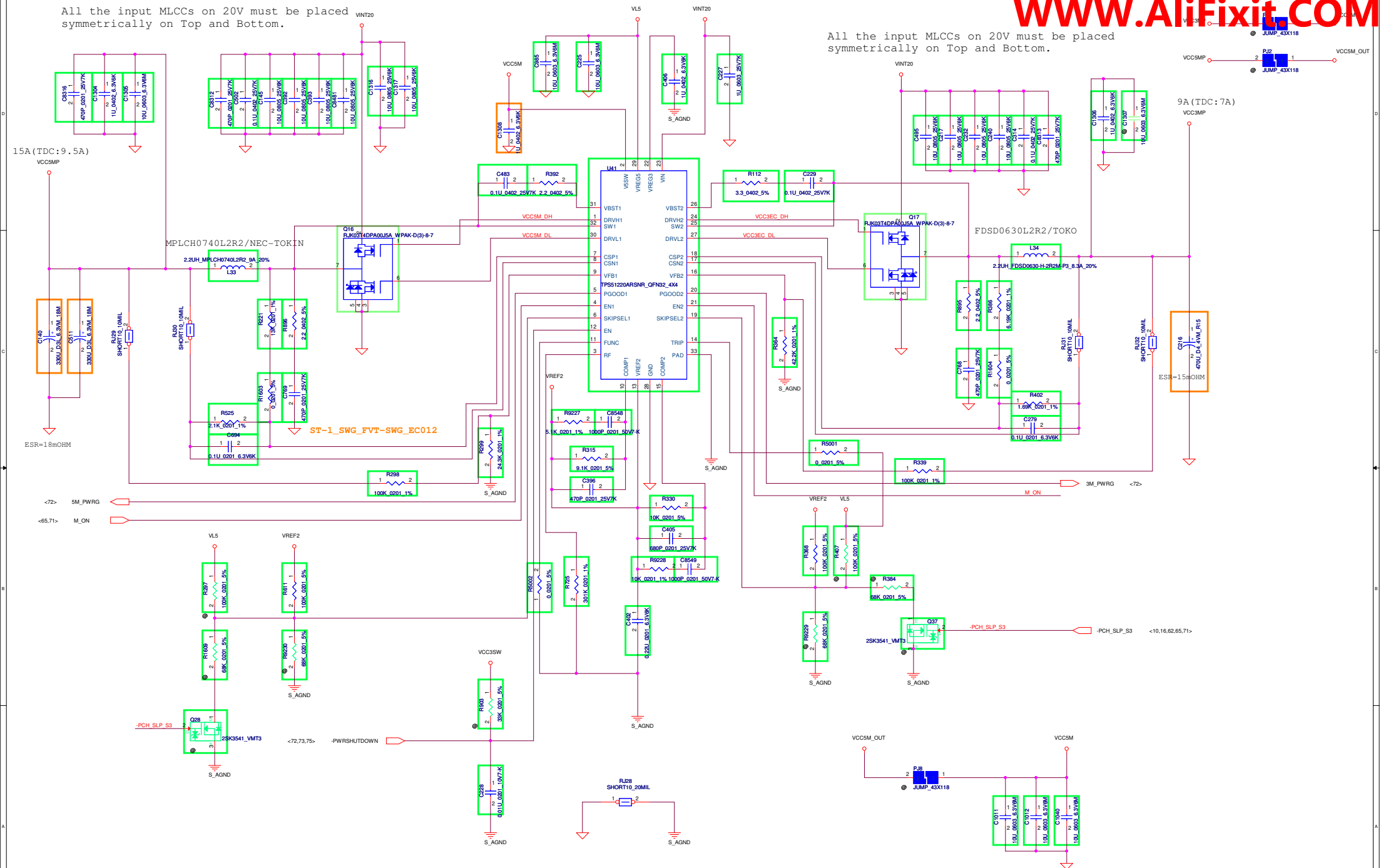
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Issued Date		2012/11/01		Deciphered Date		2013/12/31		Document Number		Cobain SWG		Rev	
Date		Tuesday, July 30, 2013		Sheet		76		of		100		0.24	

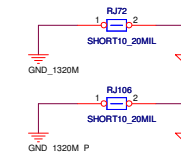



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		Document Number		Cobain SWG		Rev 0.24	
Date		Tuesday, July 30, 2013		Sheet 77		of 100	

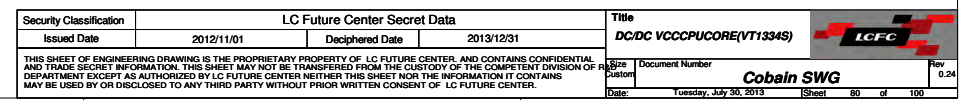
All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.






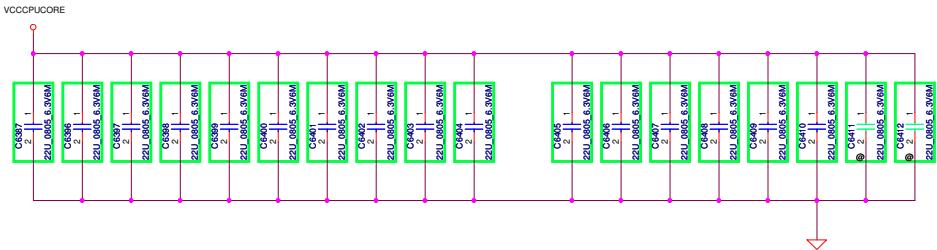
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Issued Date	2012/11/01	Deciphered Date	2013/12/31	DC/DC VCCCCPUCORE(VT1320M)			
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				[Sheet] 79 of 100			





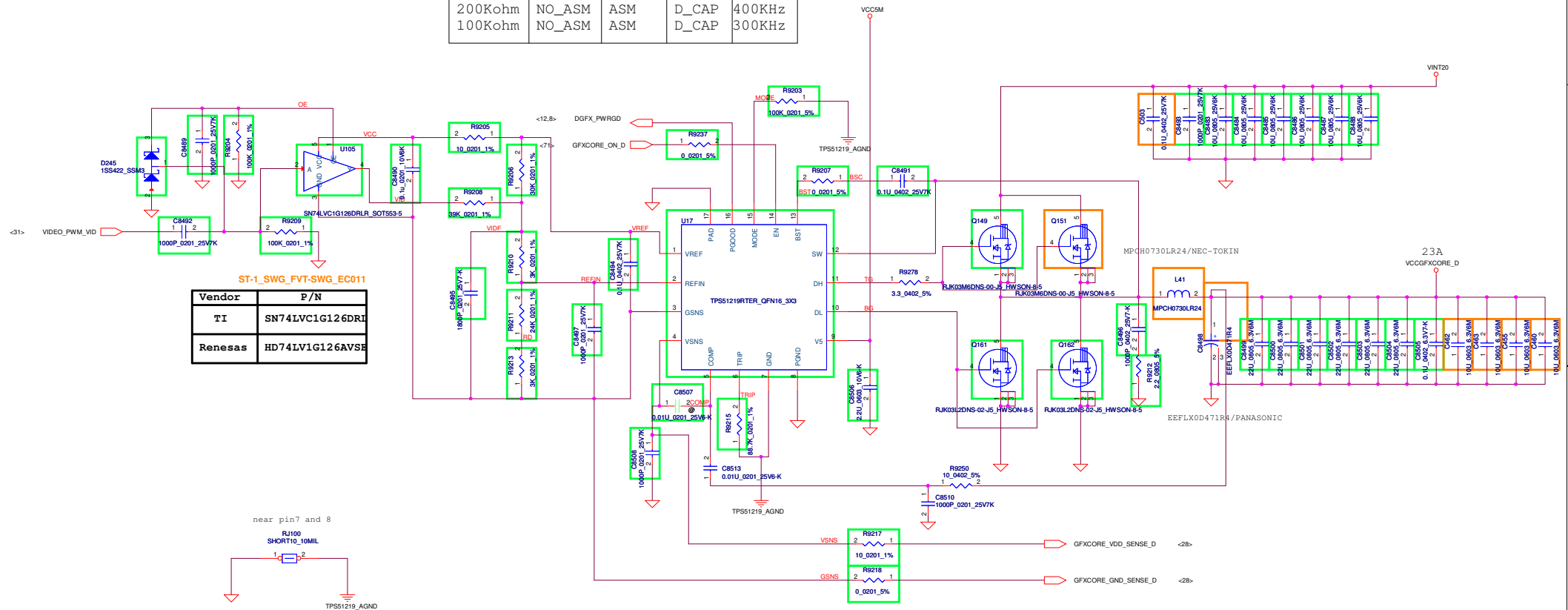
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				Date	Tuesday, July 30, 2013		



16pcs 22uF for VCCCPUCORE of 25W ULT CPU  
(14pcs 22uF for VCCCPUCORE of 15W ULT CPU)

R9203	C8507	C8513	mode	sw freq
1Kohm	ASM	NO_ASM	D_CAP2	500KHz
200Kohm	NO_ASM	ASM	D_CAP	400KHz
100Kohm	NO_ASM	ASM	D_CAP	300KHz



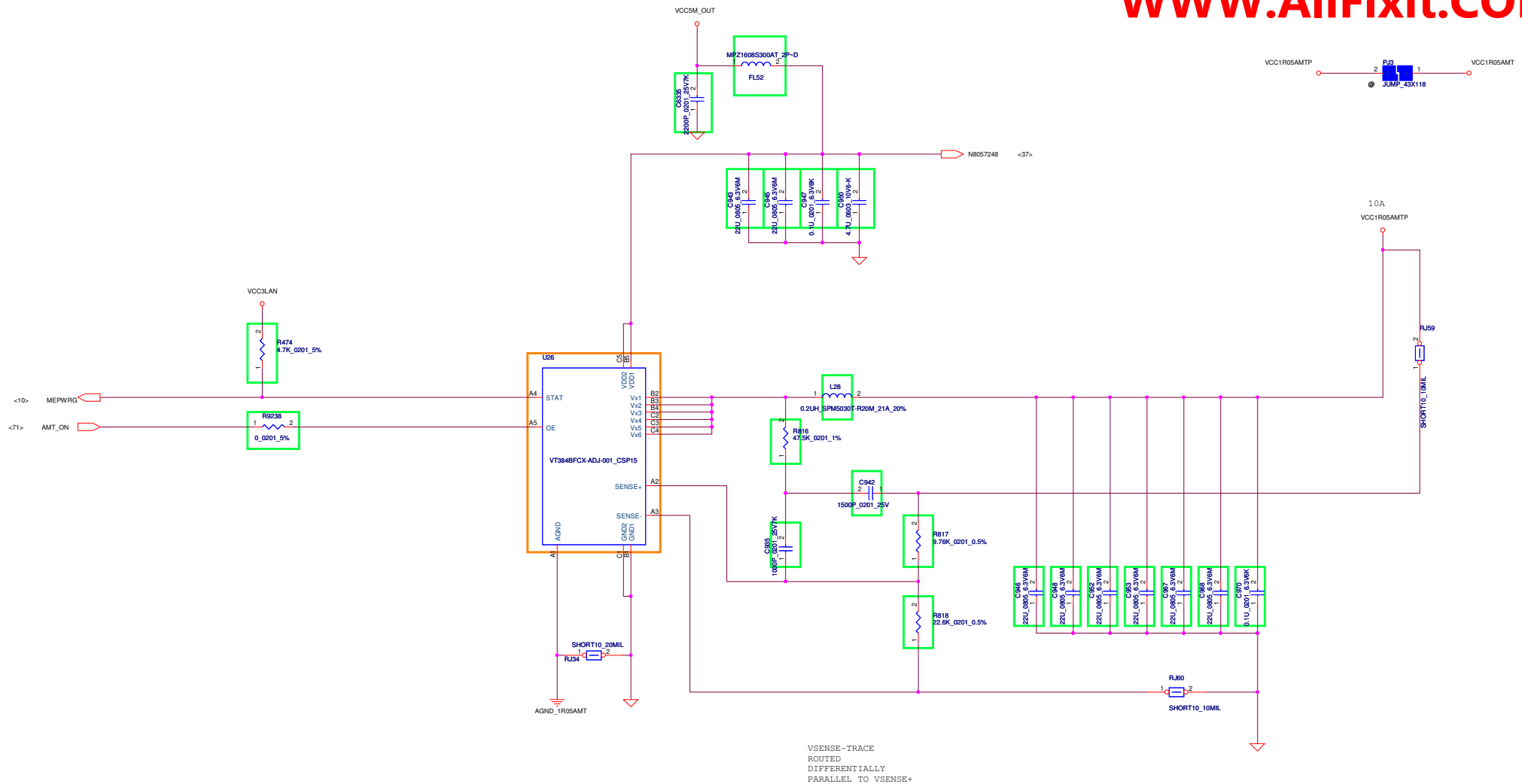
Vendor	P/N
TI	SN74LVC1G126DRL
Renesas	HD74LV1G126AVSE

Security Classification	LC Future Center Secret Data		Title
Issued Date	2012/11/01	Deciphered Date	2013/12/31
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Revision	Document Number	Cobain SWG	
Date	Tuesday, July 30, 2013	Sheet	83 of 100

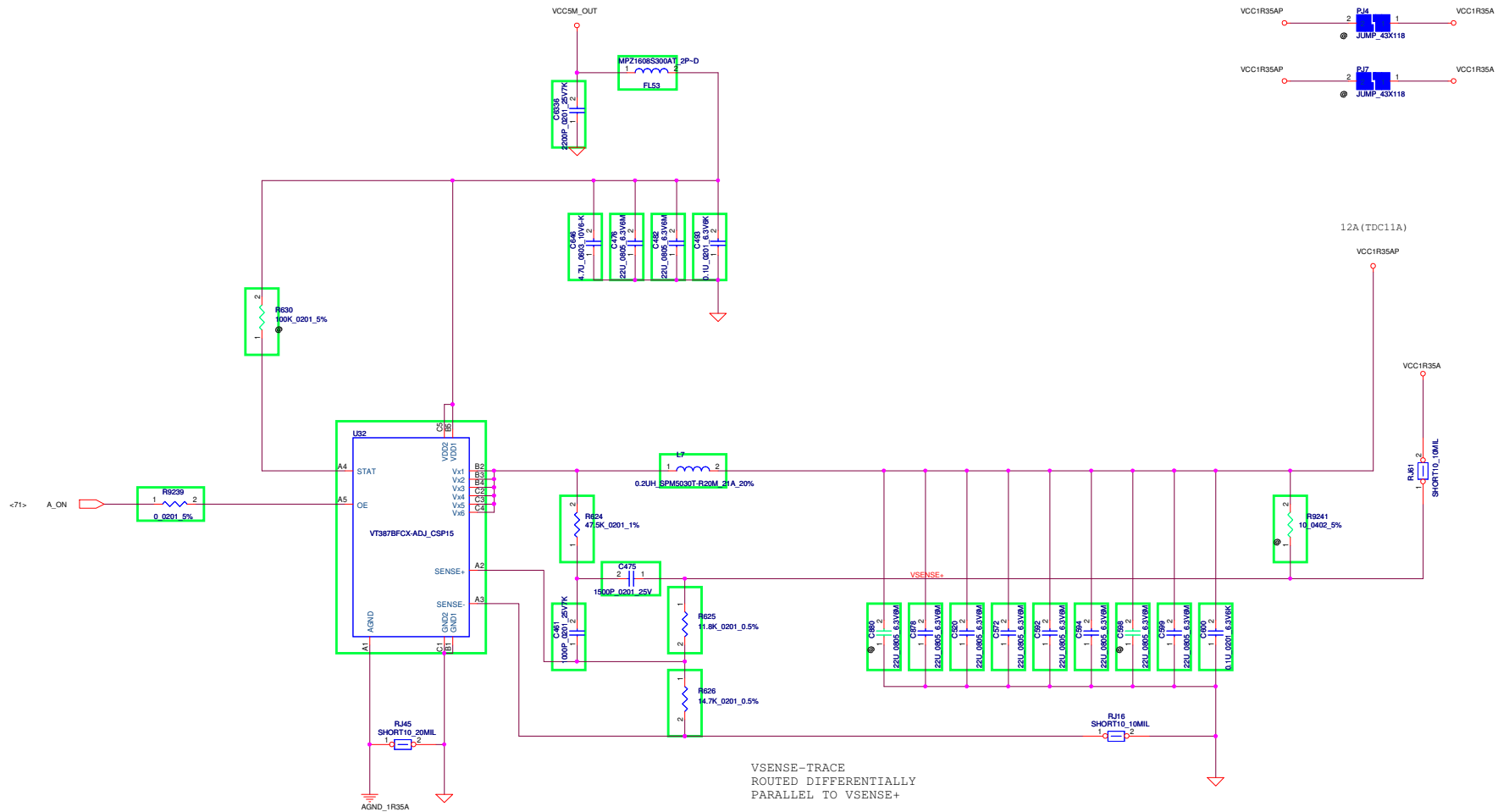
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				Cobain SWG	
Date		Tuesday, July 30, 2013		Sheet 84 of 100	





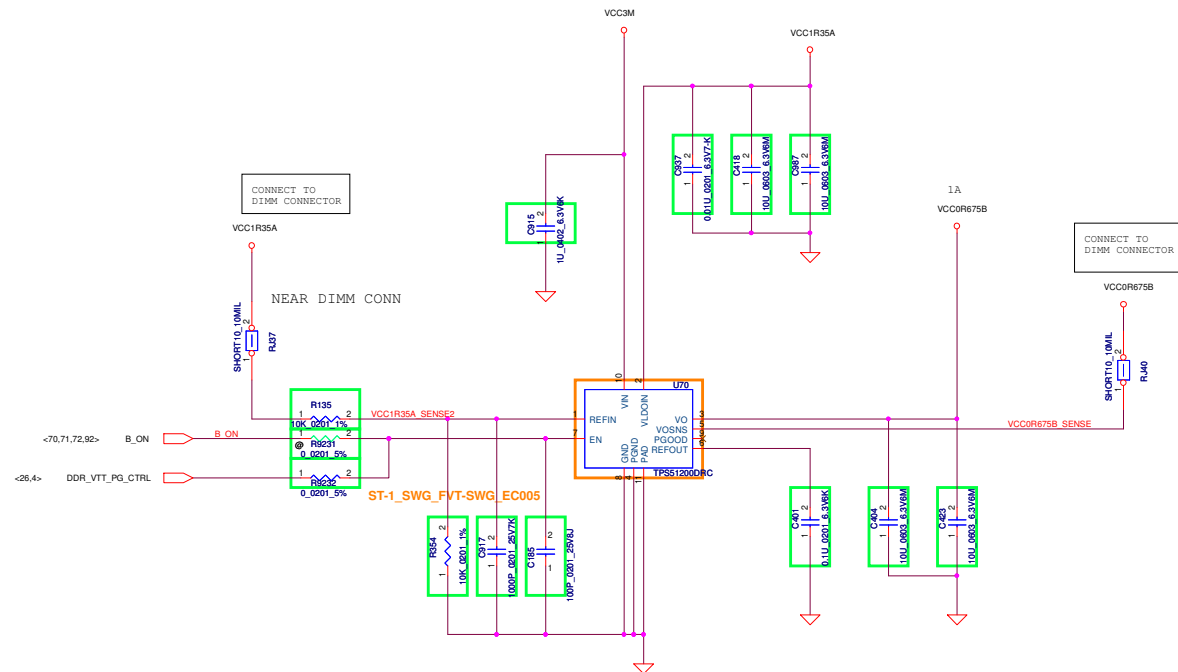
$$V_{out} = 0.75 \times (1 + R_{817}/R_{818})$$



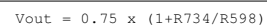
$$V_{out} = 0.75 \times (1 + (R_{F1}/R_{F2}))$$


RF1 RF2  
3.65K 4.53K for 1.35V  
4.02K 4.02K for 1.50V

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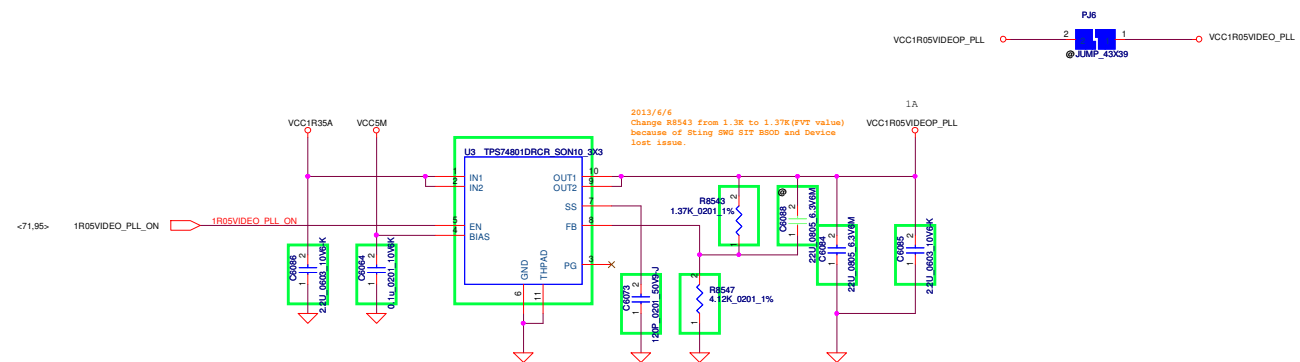



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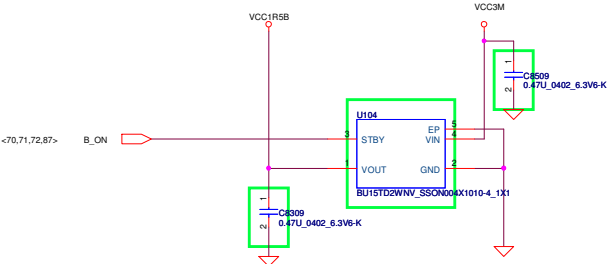
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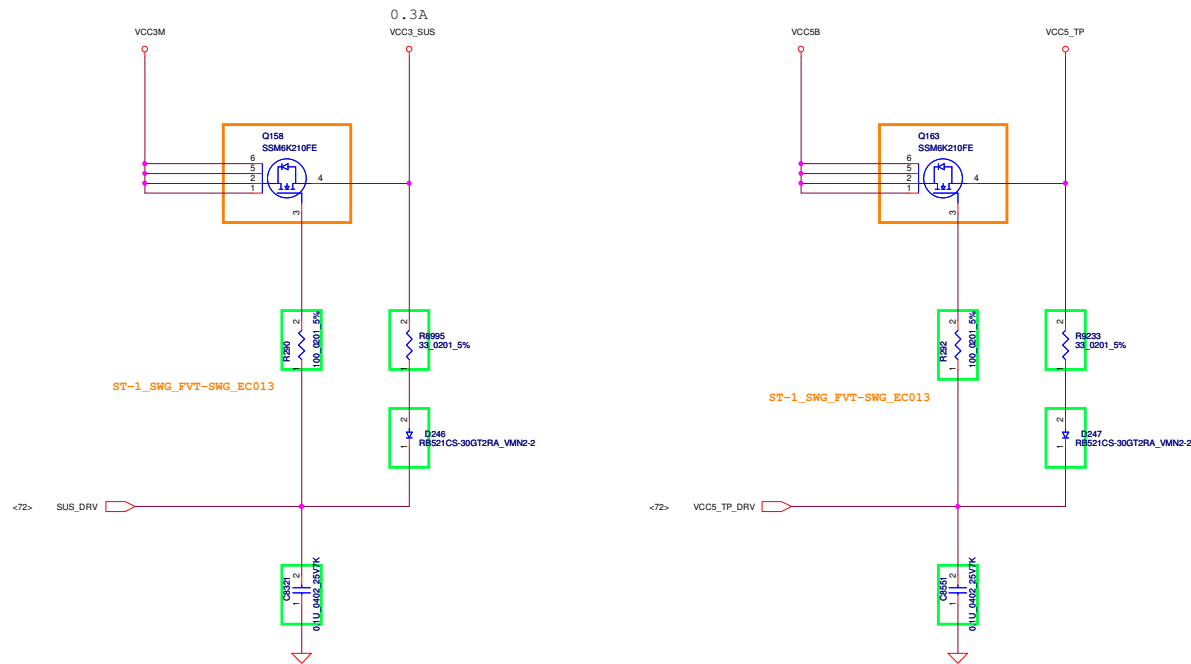
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Date: Tuesday, July 30, 2013				Sheet	91 of 100

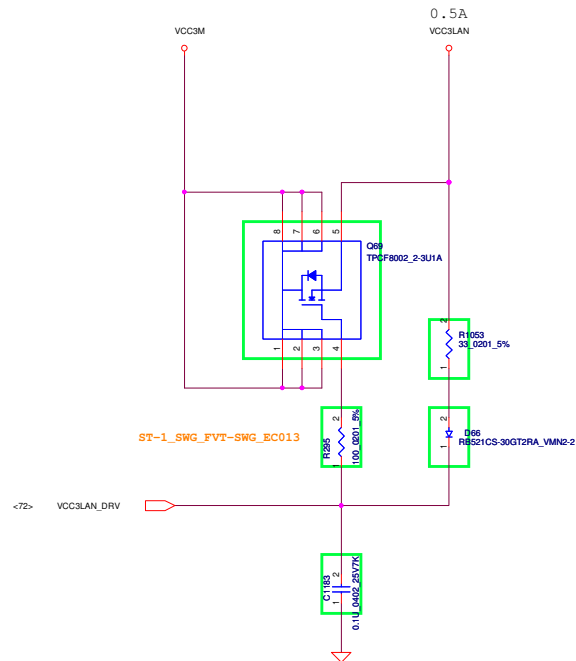





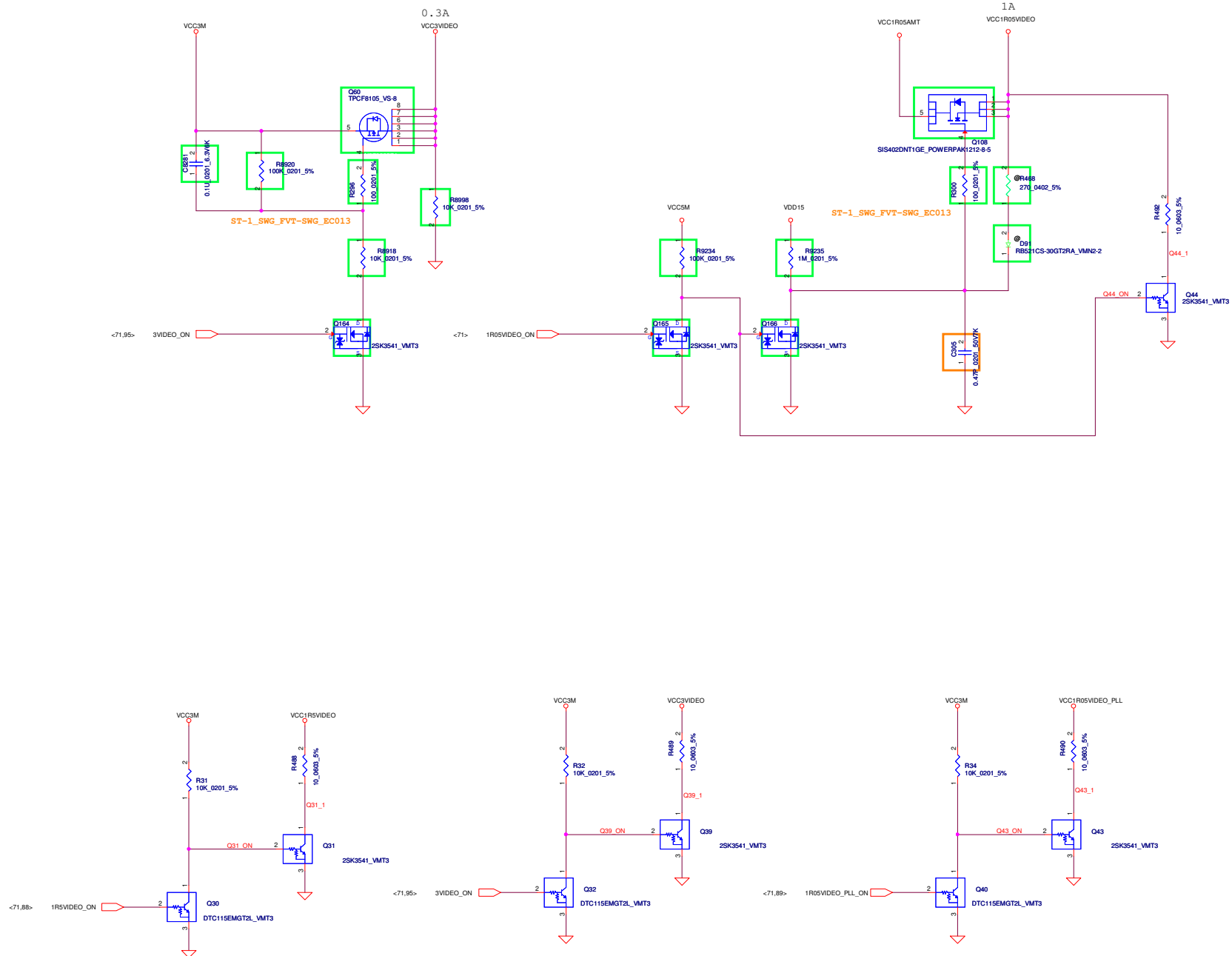
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				Date	Tuesday, July 30, 2013
				Sheet	92 of 100



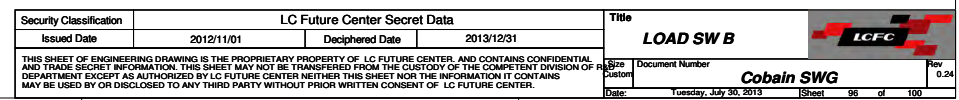
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Date: Tuesday, July 30, 2013					0.24
Sheet 93 of 100					



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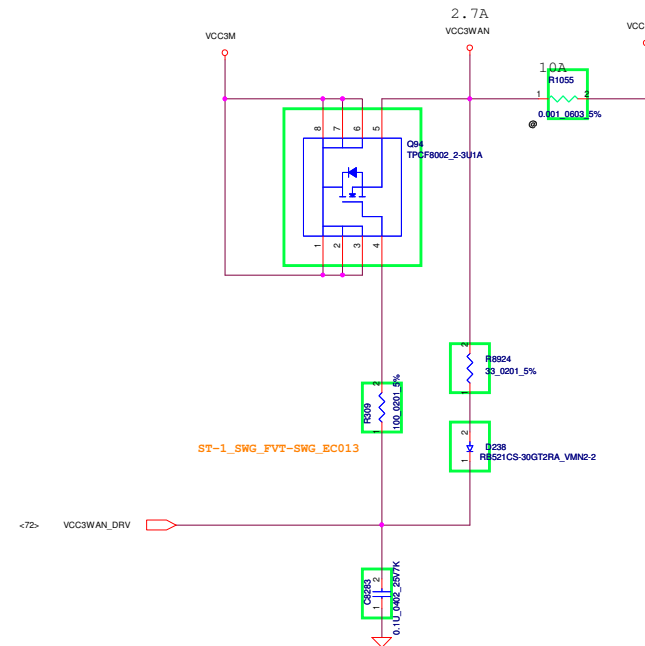






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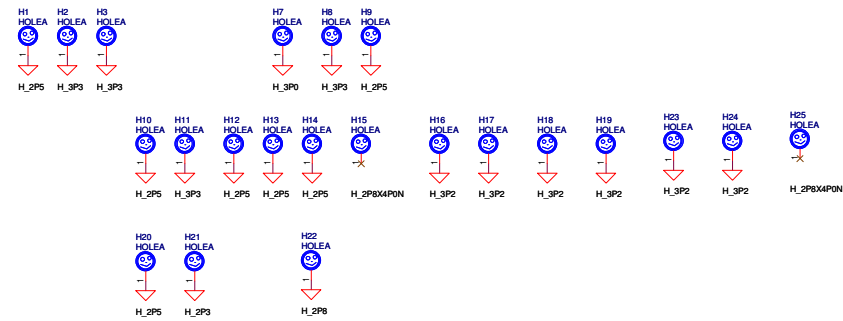
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				Cobain SWG	
Date: Tuesday, July 30, 2013				Sheet	97 of 100





AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
R8926	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

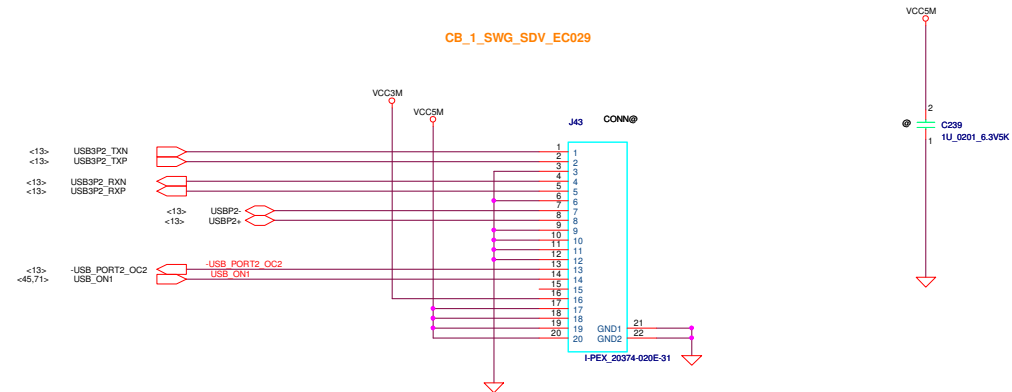
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					Rev 0.24
					Sheet 98 of 100



FID  
Board Area

FID  
Component Area

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Rev 0.24